

CRESCENT
MV

2019.03.27

Marking	Description
I	Install
NI	Non-install
PROTO	Proto type
MP	Mass Production
TAA	Install for TAA
CRITICAL	Critical Parts

21-OCT-2002		
DATE	CHANGE NO.	REV

DESIGN/DRAWER				DATE				21-OCT-2002			
CHECK				XXX				21-OCT-2002			
APPROVAL				MORRIS CHANG							
FILE NAME				IHS03011-000A10000-MB.A2							
PCB PIN				50XXXXXXXXXX				PCB VER XXX			
TITLE				MODEL,PROJECT,FUNCTION				MAIN BOARD			
SIZE				A3				CODE			
SHEET				1				DOC NUMBER			
								1310XXXX-0-0			
								REV			
								201			

INVENTEC

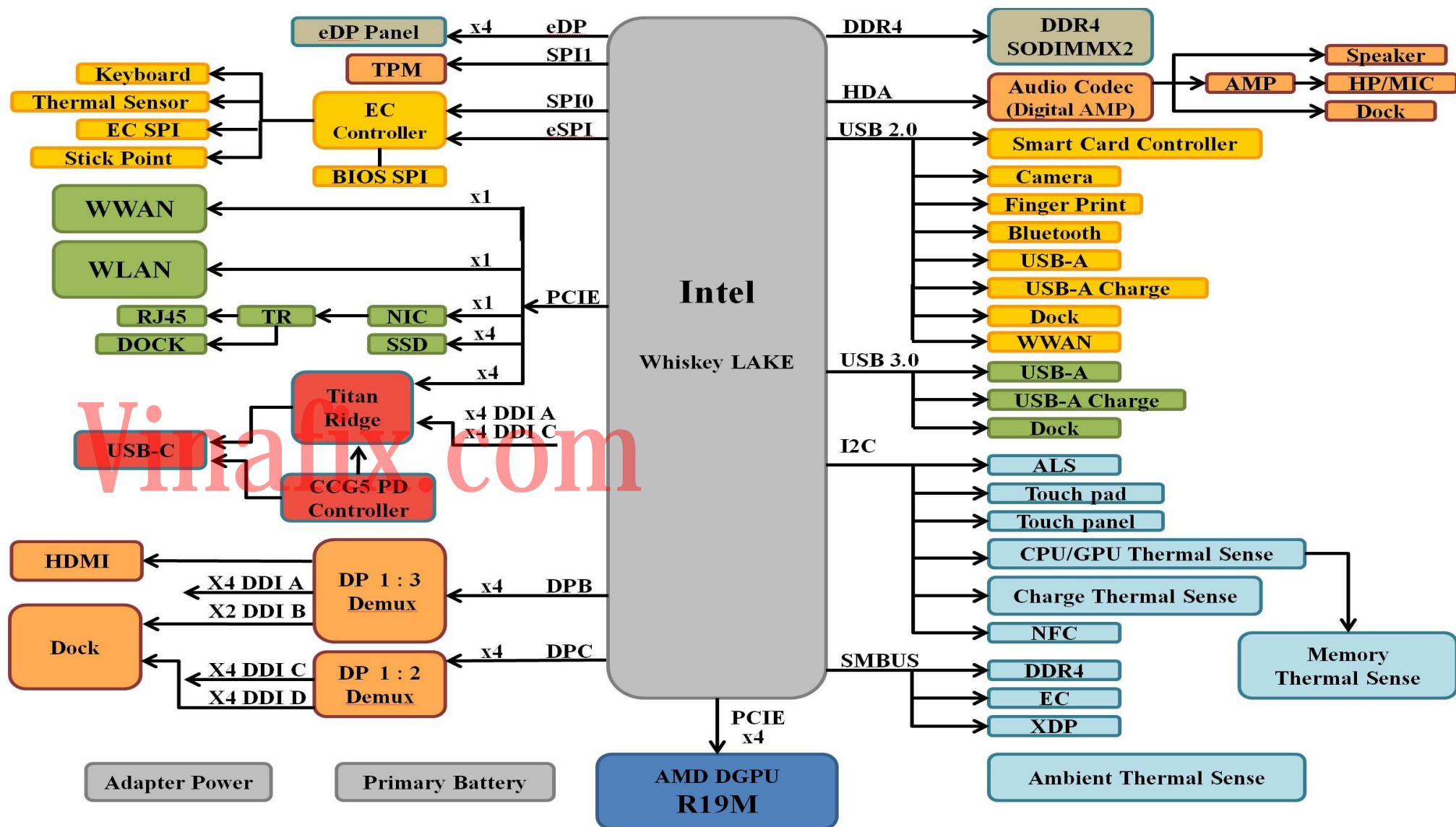
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35. XDP & ME CONN.	71. WWAN NGFF	
36. DEBUG CONN	72. DOCKING	

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TITLE MODEL PROJECT,FUNCTION
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SHEET 2 of 105							



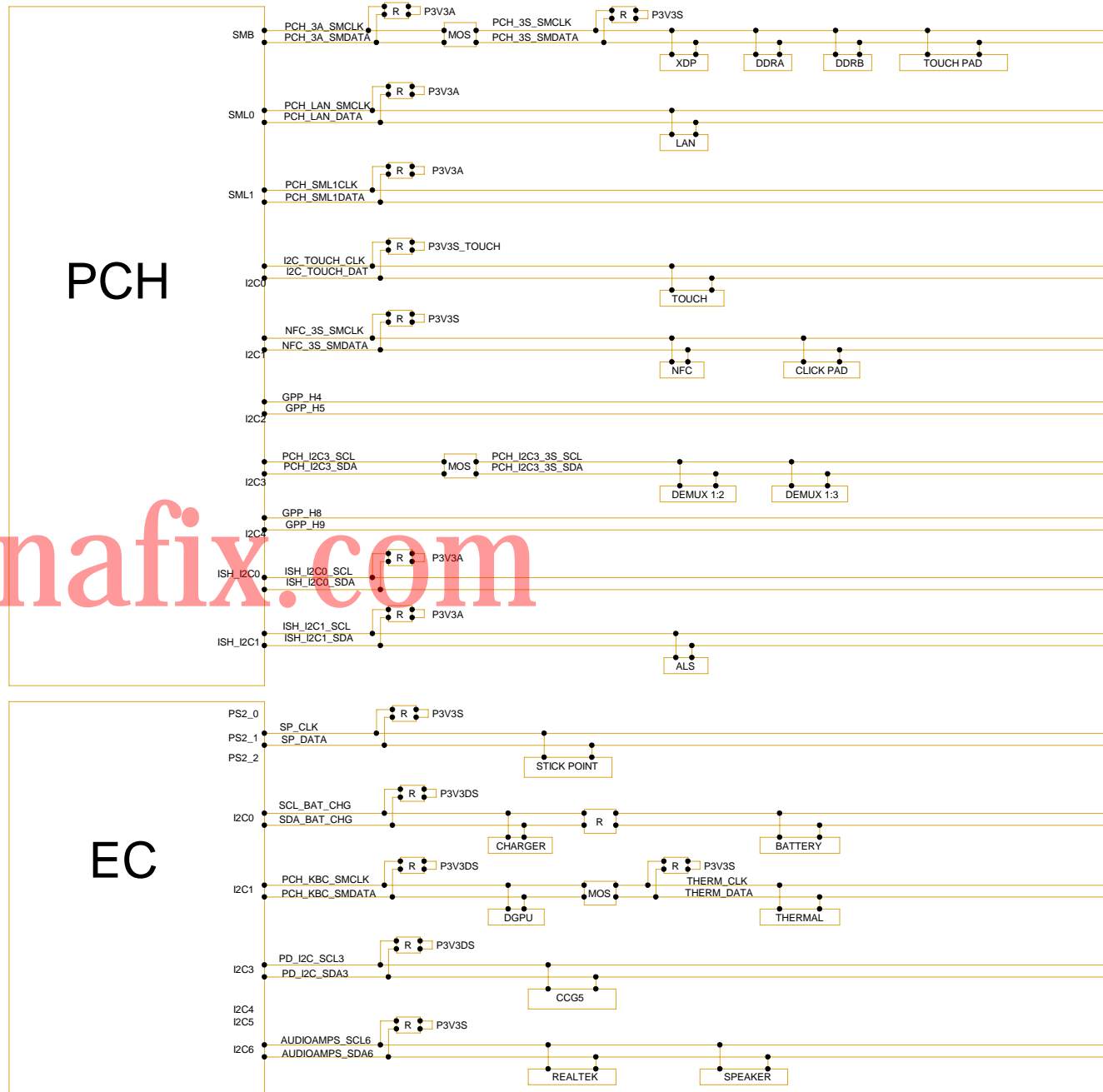
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TITLE
MODEL PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

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CHANGE BY XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

**INVENTEC**

TITLE			
MODEL,PROJECT,FUNCTION			
POWER BLOCK DIAGRAM			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310XXXX-0-0	201
SHEET	4	#	USE

SIGNAL	VOLTAGE	G3	S5	S3	S0
RTC	3.3V	O	O	O	O
PVBAT	12V	X	O	O	O
P3V3DS	3.3V	X	O	O	O
P3V3A	3.3V	X	O	O	O
P3V3S	3.3V	X	X	X	O
P3V3S_TP	3.3V	X	X	X	O
P5V0DS	5V	X	O	O	O
P5V0S	5V	X	X	X	O
P1V05A	1.05V	X	O	O	O
P1V2	1.2V	X	X	O	O
P2V5	3.3V	X	X	O	O
P1V8DS	1.8V	X	O	O	O
P1V5S	1.5V	X	X	X	O
PVCCIO	0.95V	X	X	X	O
PVCC_PRIM	1.05V	X	O	O	O
PVCORE	SVID	X	X	X	O
PVCCGT	SVID	X	X	X	O
PVCCSA	1V	X	X	X	O
PVCCSFR	1.05V	X	X	O	O
PVCORE_DGPU	SVID	X	X	X	O
P1V3SS_DGPU	1.35V	X	X	X	O
PVDDCI_DGPU	SVID	X	X	X	O
P1V8S_DGPU	1.8V	X	X	X	O

STACK_UP for 8 layer-0.9mm-5Signal

Top		0.60mil 1.55mil 2.70mil	(Solder Mask) (Hoz + Plating)	1 OZ min
L2	P/P 2.7mil		(GND)	H OZ
L3	CORE 4mil	0.60mil 4.00mil	(SIGNAL)	H OZ
L4	P/P 4.4mil	0.60mil 4.40mil	(VCC)	1 OZ
L5	CORE4mil	1.30mil 4.00mil	(SIGNAL)	1 OZ
L6	P/P 4.4mil	1.30mil 4.40mil	(SIGNAL)	H OZ
L7	CORE 4mil	0.60mil 4.00mil	(GND)	H OZ
Bottom	P/P 2.7mil	0.60mil 2.70mil	(Hoz + Plating) (Solder Mask)	1 OZ min
		ideal: 35.50mil 0.90mm		

Base-U Port	Coronado 14/15-WHL
USB30_P1	USB Type A(Left)
USB30_P2	USB Type A(Right)
USB30_P3	WWAN(PCIE)
USB30_P4	Dock (3.1 Gen1)
PCle5	TBT
PCle6	TBT
PCle7(GbE)	LAN
PCle8(GbE)	WLAN
PCle9 (GbE)	dGPU
PCle10	dGPU
PCle11 /SATA 0	dGPU
PCle12 /SATA 1A	dGPU
PCle13 (GbE)	SSD(NVMe)
PCle14 (GbE)	SSD(NVMe)
PCle11	SSD(NVMe)
PCle12	SSD(NVMe)/SATA SSD

USB2		
1	USB 2.0 #1	USB Type A(Left)
2	USB 2.0 #2	USB Type A(Right)
3	USB 2.0 #3	WWAN (USB2.0)
4	USB 2.0 #4	USB Dock
5	USB 2.0 #5	Type C
6	USB 2.0 #6	RFID
7	USB 2.0 #7	Smart Card
8	USB 2.0 #8	Finger Print Reader
9	USB 2.0 #9	Camera
10	USB 2.0 #10	WLAN/BT

PLT_ID1	PLT_ID2	PLT_ID3	ALS_DETECT#	
0	1	0	X	CRESCENT 14" VPRO
0	1	1	X	CRESCENT 15" VPRO
1	1	0	X	CRESCENT 14" NON-VPRO
1	1	1	X	CRESCENT 15" NON-VPRO
X	X	X	1	CRESCENT NON-ALS
			0	CRESCENT ALS

NOTE : DEFAULT MB IS DIS , 15" , VPRO , NON-ALS SKU

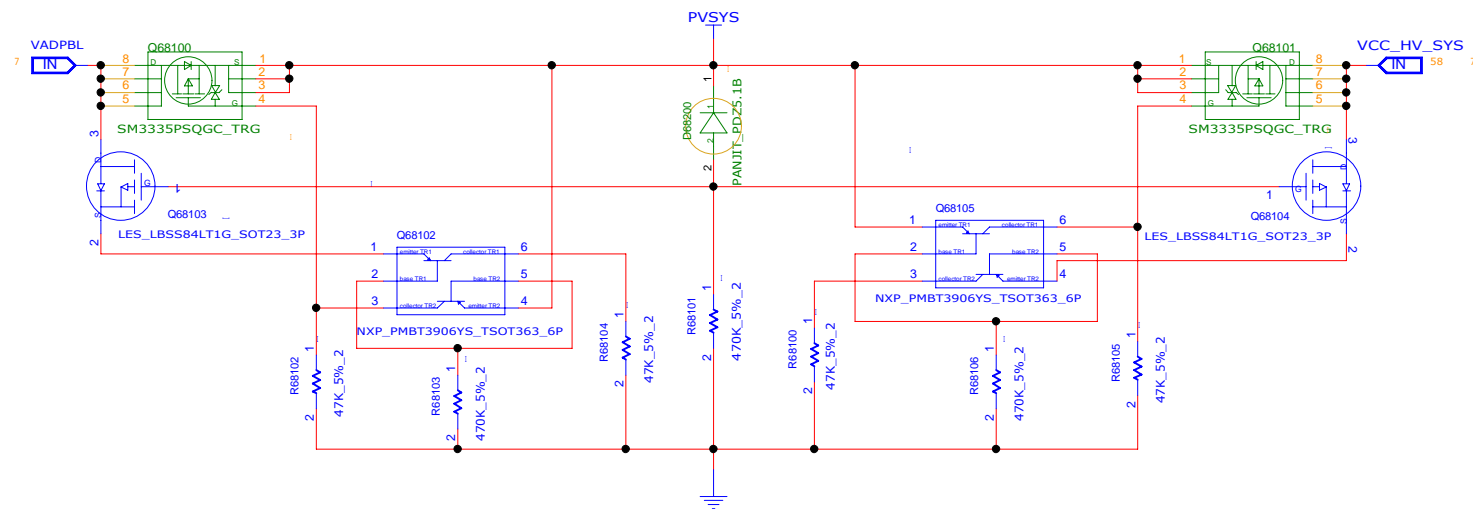
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
	0	0	1	1
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
	0	1	1	1
SI3	1	0	0	0
PV	1	0	0	1
PVR	1	0	1	0
	1	0	1	1
MV	1	1	0	0

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TITLE	MODEL,PROJECT,FUNCTION	DESIGN INFORMATION
SIZE A3	CODE CS	DOCNUMBER 1310xxxx-0-0
SHEET 1	REV 001	

CHANGE#	XXX	DATE	21-OCT-2002
PCB.PIN	XXXXXXXXXX	PCB.VER	XXX





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TITLE
MODEL PROJECT FUNCTION
BARREL/PO SELECT

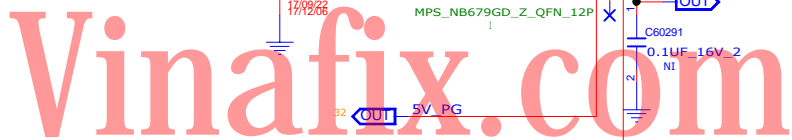
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SHEET		8 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



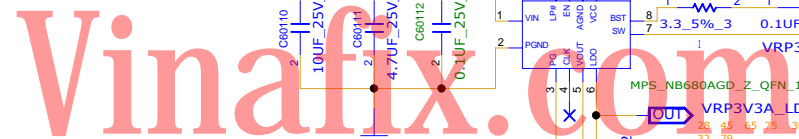
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SHEET		9 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		10 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION P3V3DS (NB680A)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 11 of 105			



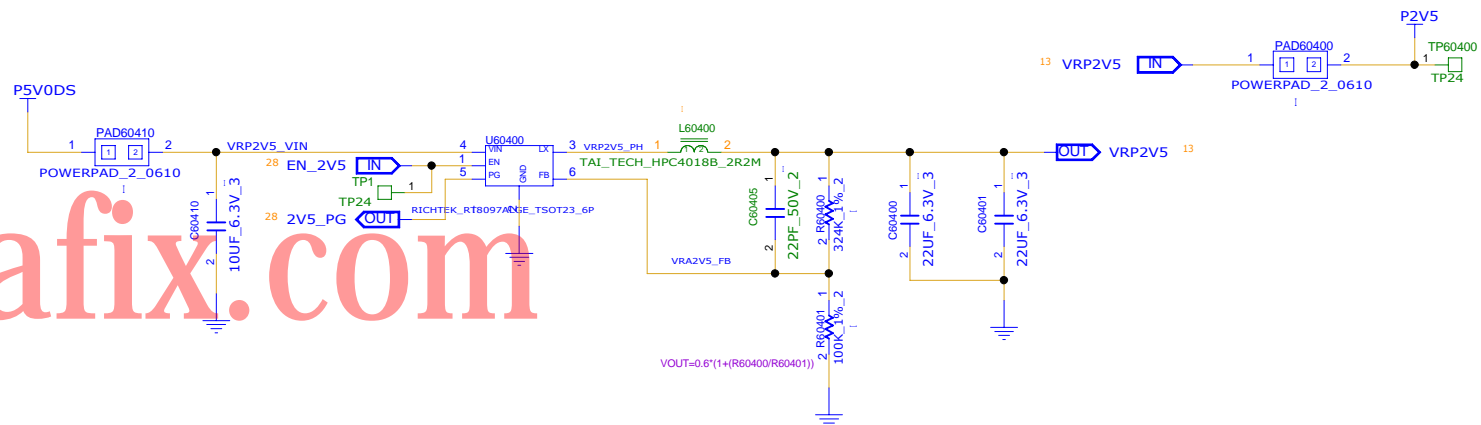
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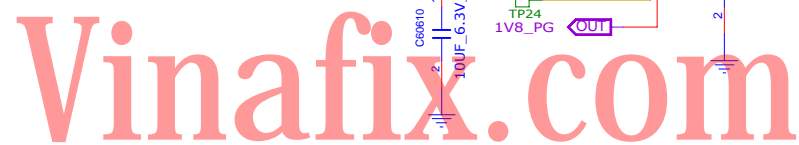


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TITLE
MODEL, PROJECT, FUNCTION
P2V5 - (RT8097A)

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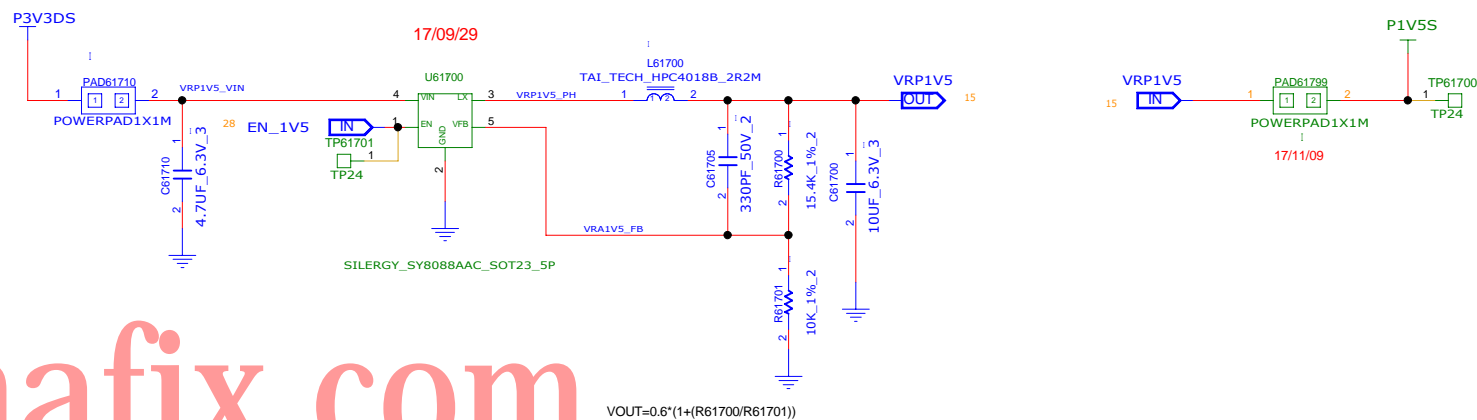
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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$$V_{OUT} = 0.6 * (1 + (R_{60600} / R_{60601}))$$

17/11/09

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		14 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



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TITLE
MODEL, PROJECT, FUNCTION
P1V5 (SY8088AAC)

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

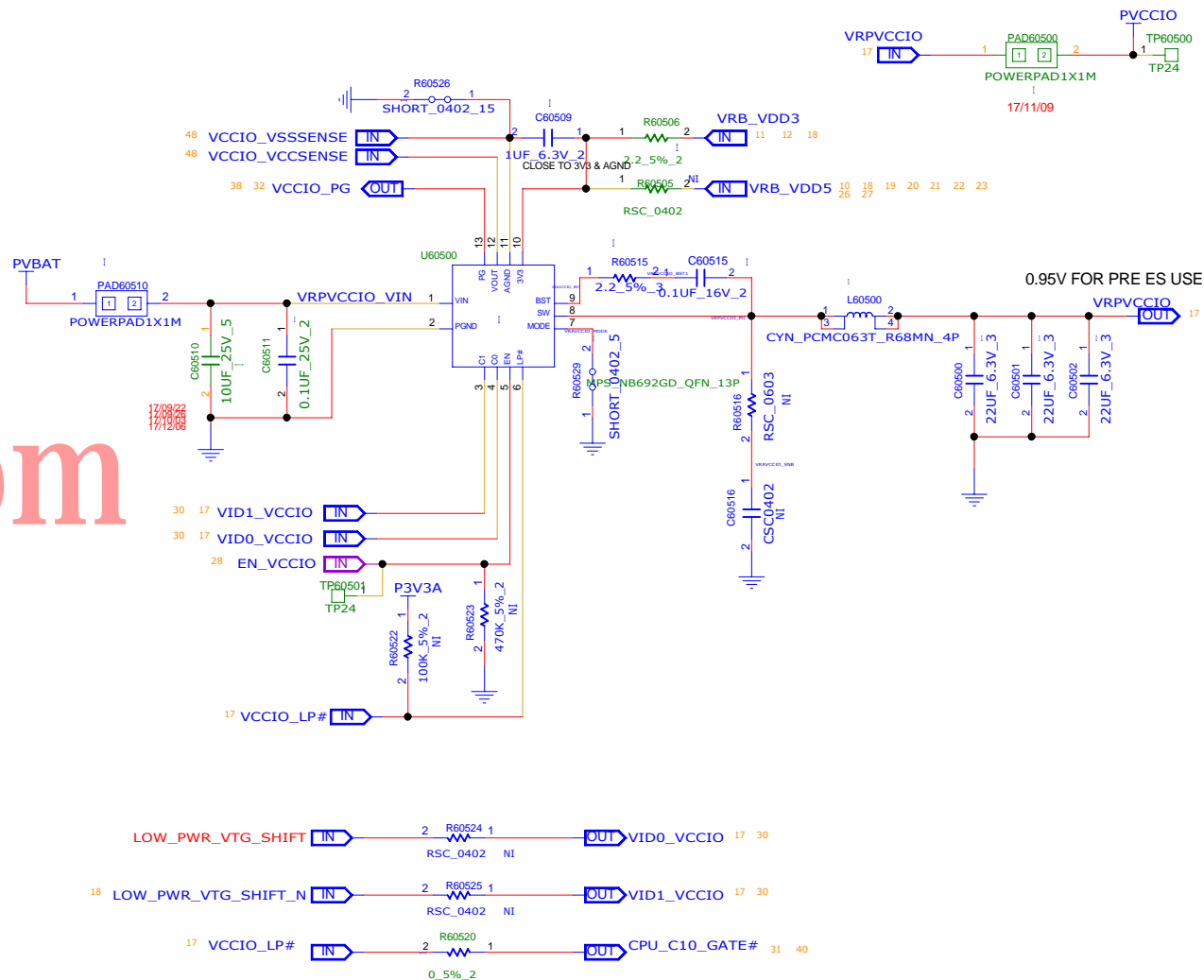
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.75
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1.0
	1	1	1	1.05
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5
	1	1	1	2.5



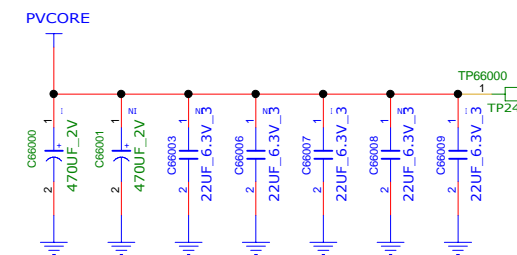
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TITLE			
MODEL PROJECT FUNCTION PVCIO (NB692GD)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 17 of 105			

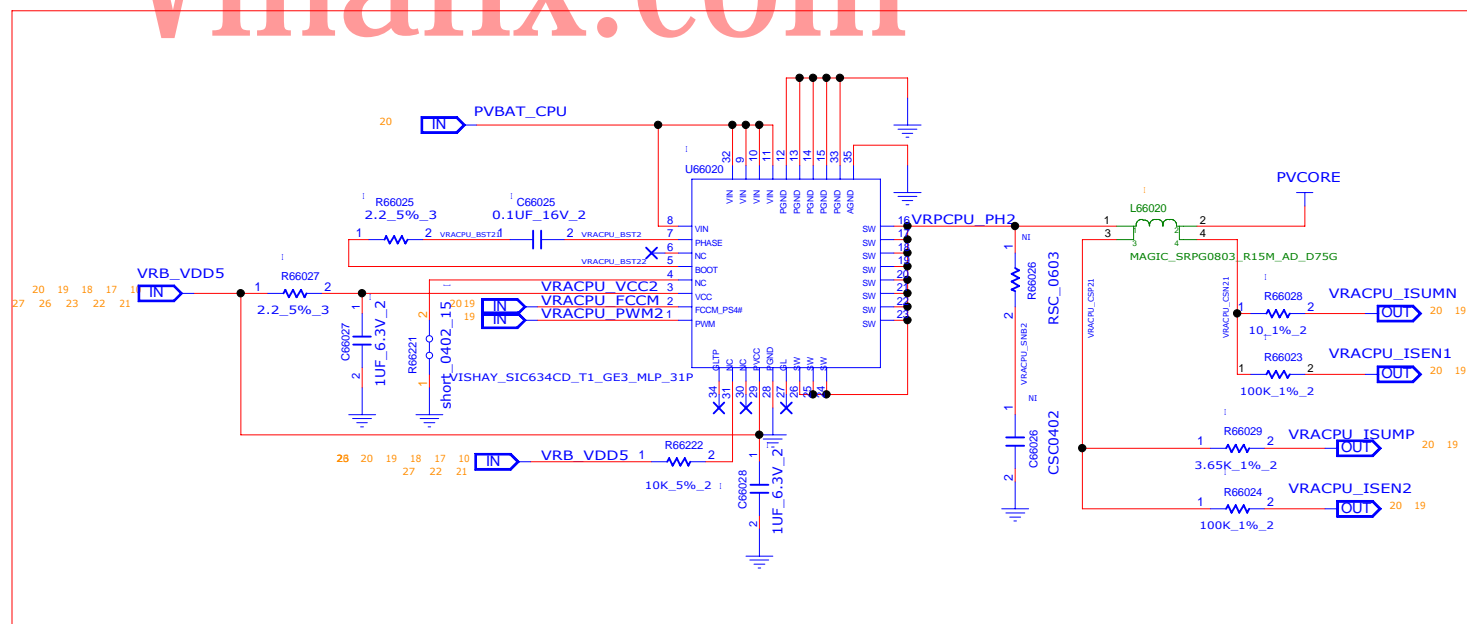
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



TDC=48A
MAX=70A

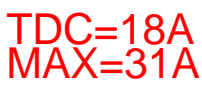


NOTE:NOT INSTALL FOR U22

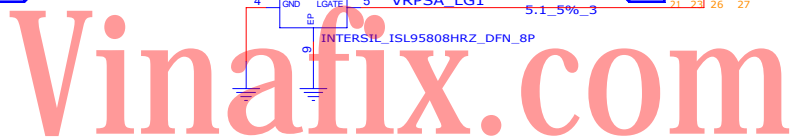


SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	R X
SHEET		20 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



TDC=6A
MAX=20A

<h1>INVENTEC</h1>			
TITLE MODEL,PROJECT,FUNCTION PVCCSA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 22 of 105			

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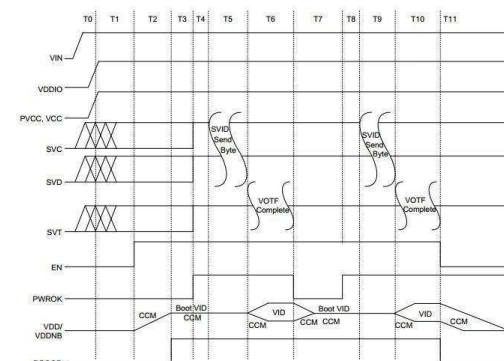
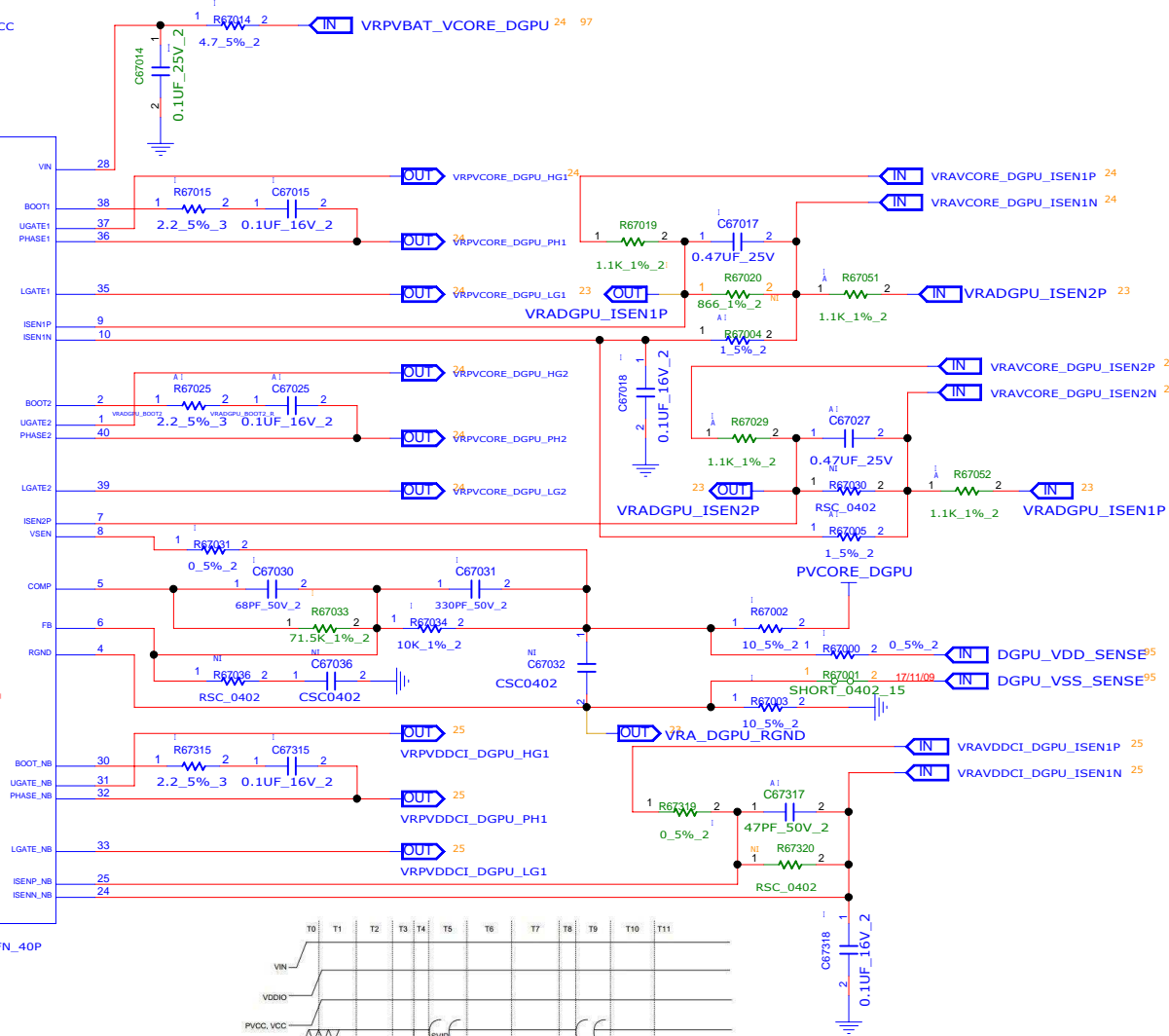
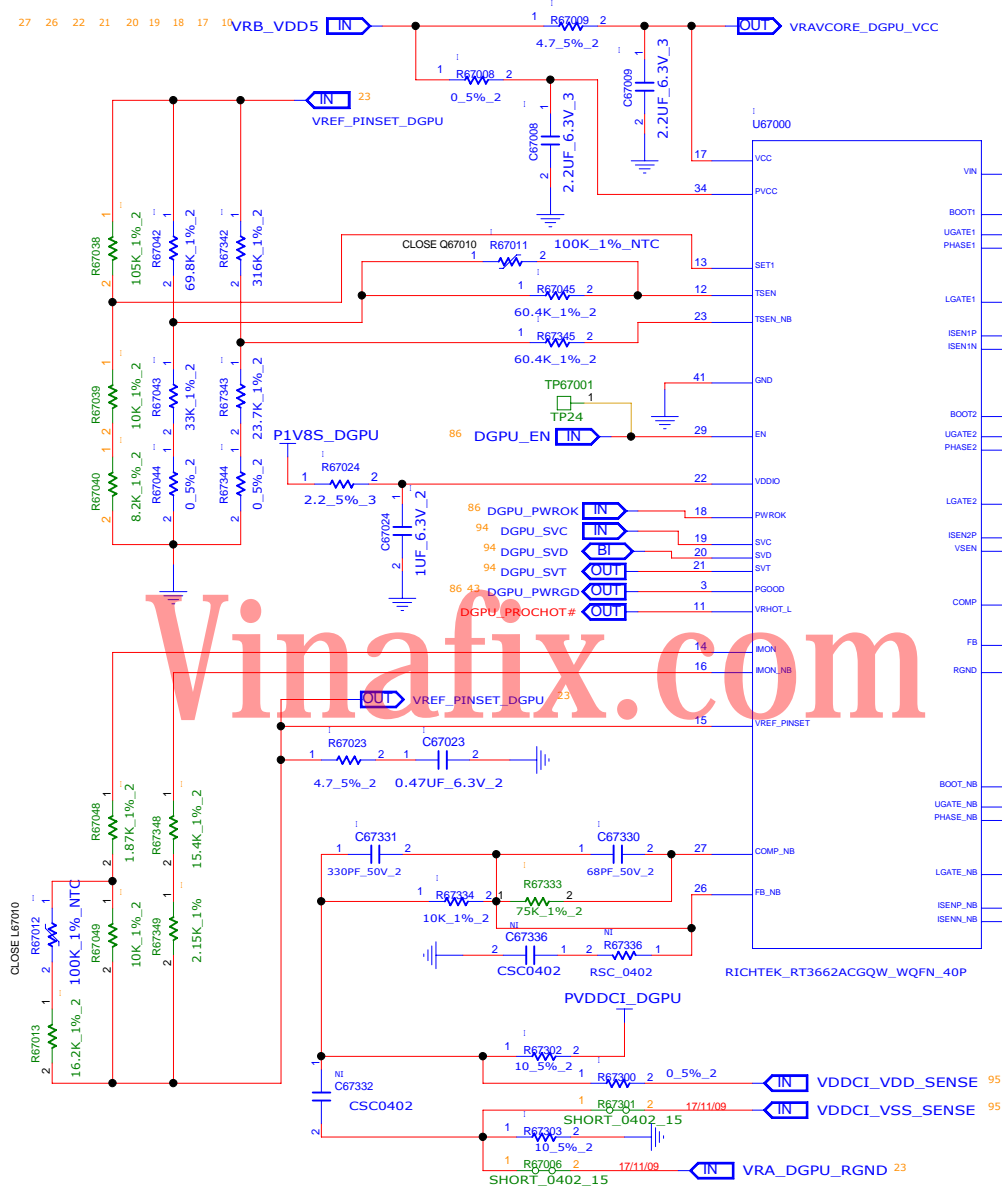


Figure 2. Simplified Sequence Timing Diagram

Table 7. 2-Bit Boot VID Code

SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

NOTE : WHEN TSEN OR TSEN_NB IS LESS THEN 2.2V THE VRHOT_L WILL BE PULLED LOW.

ATI 18W_3H-01	FREQUENCY	DCR	LOAD LINE	TDC	OCP
PVCORE_DGPU	400 KHZ	1.19 MOHM	0.6 MOHM	22.0 A	70.0 A
PVDDCI_DGPU	400 KHZ	2.0 MOHM	0 MOHM	8.0 A	12.0 A

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TITLE			
MODEL PROJECT FUNCTION			
ATIDGPU_18W_VR			
SHEET	CODE CS	DOC NUMBER	REV
23 of 105	XXX	1310xxxxx-0-0	X01

CHANGE by	DATE
XXX	21-OCT-2002
PCB P/N	PCB VER
60xxxxxxxxxx	XXX



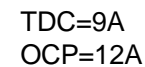
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



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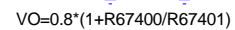
SHEET 25 of 105



TITLE	MODEL,PROJECT,FUNCTION
	P1V35S_DGPU(G5225)

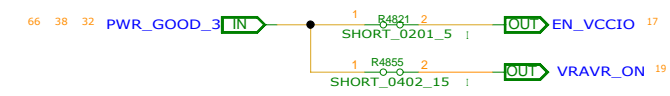
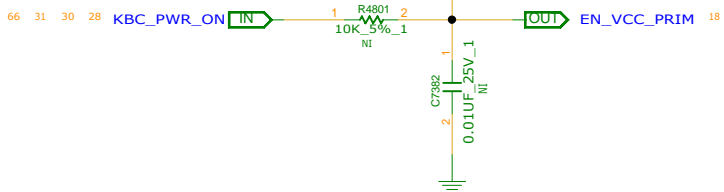
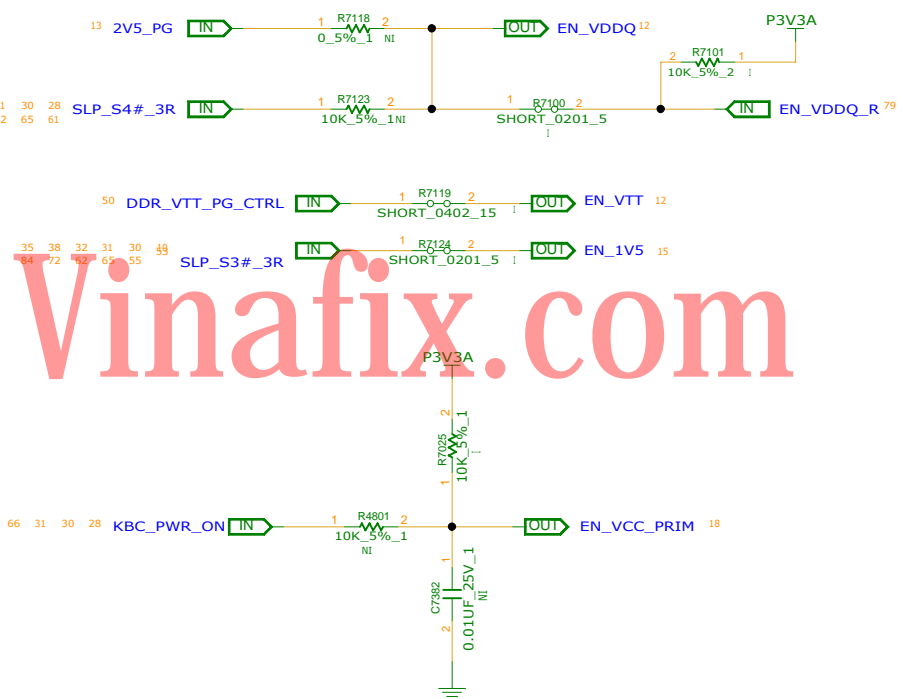
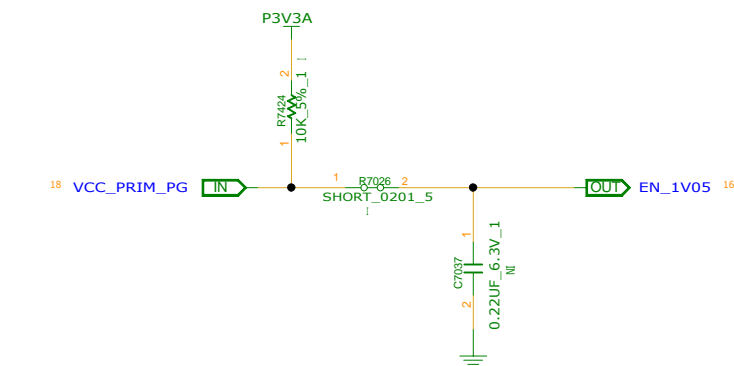
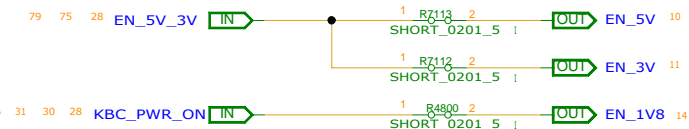
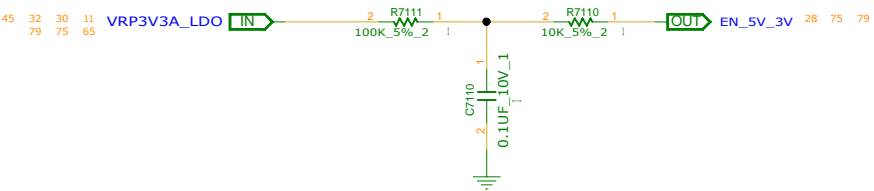
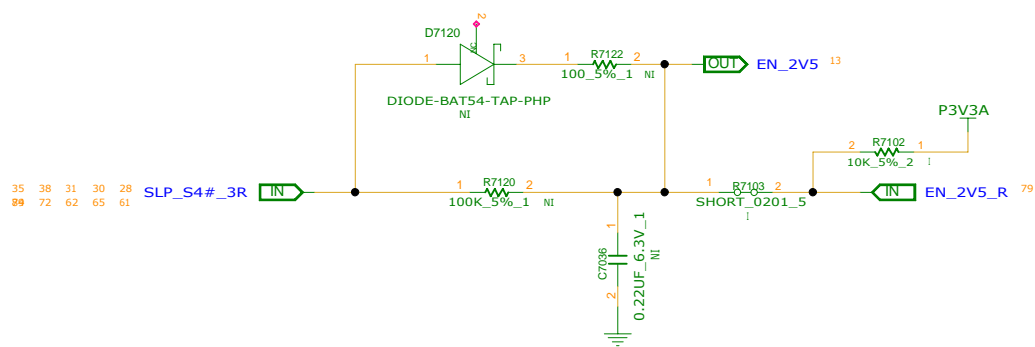
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	F X
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		27 of 105	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



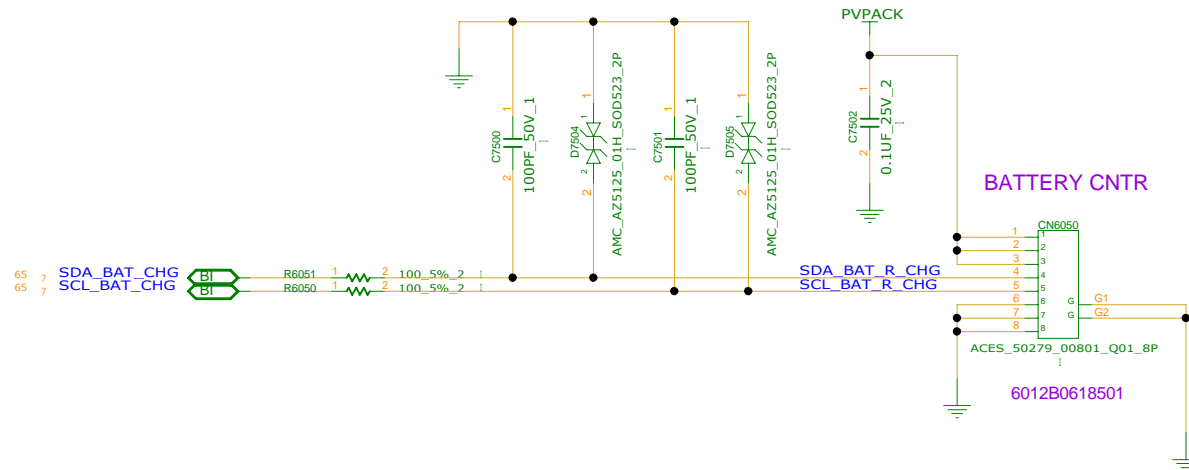
POWER ENABLE SIGNAL

POWER TO EE NET NAME CONNECTION

LOCATION NUMBER : 7000~7499

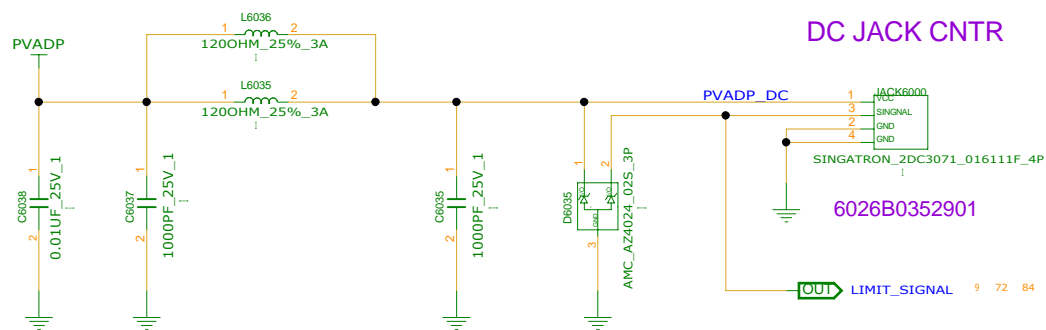
INVENTEC			
TITLE MODEL PROJECT FUNCTION POWER ENABLE SIGNALS			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 28 of 105			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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LOCATION NUMER : 6050~6099

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LOCATION NUMER : 6000~6049

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TITLE
MODEL PROJECT FUNCTION
DC JACK & BATT. CNTR

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 29 of 105			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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POWER SEQUENCE(P3V3S,P5V0S)

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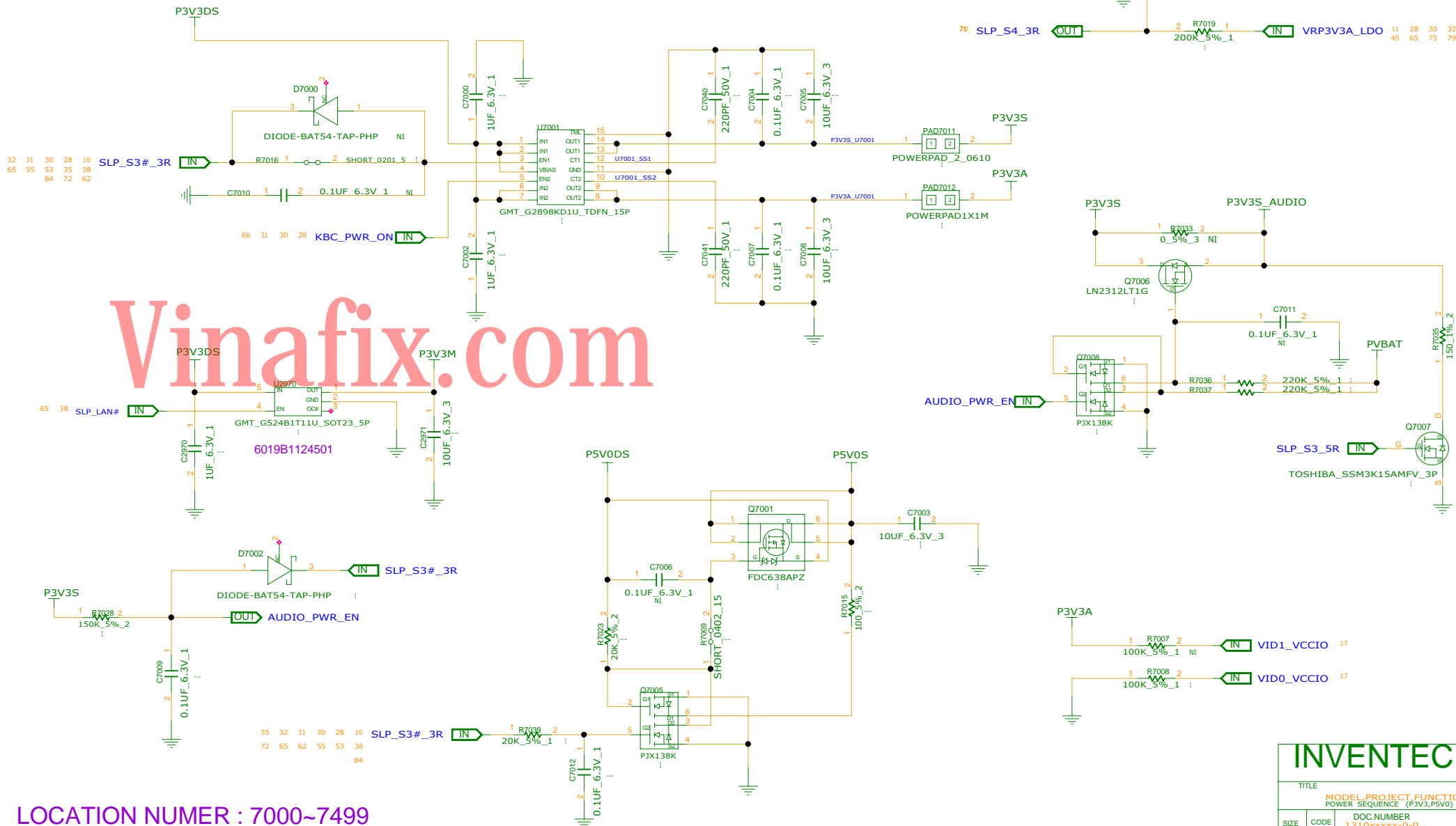
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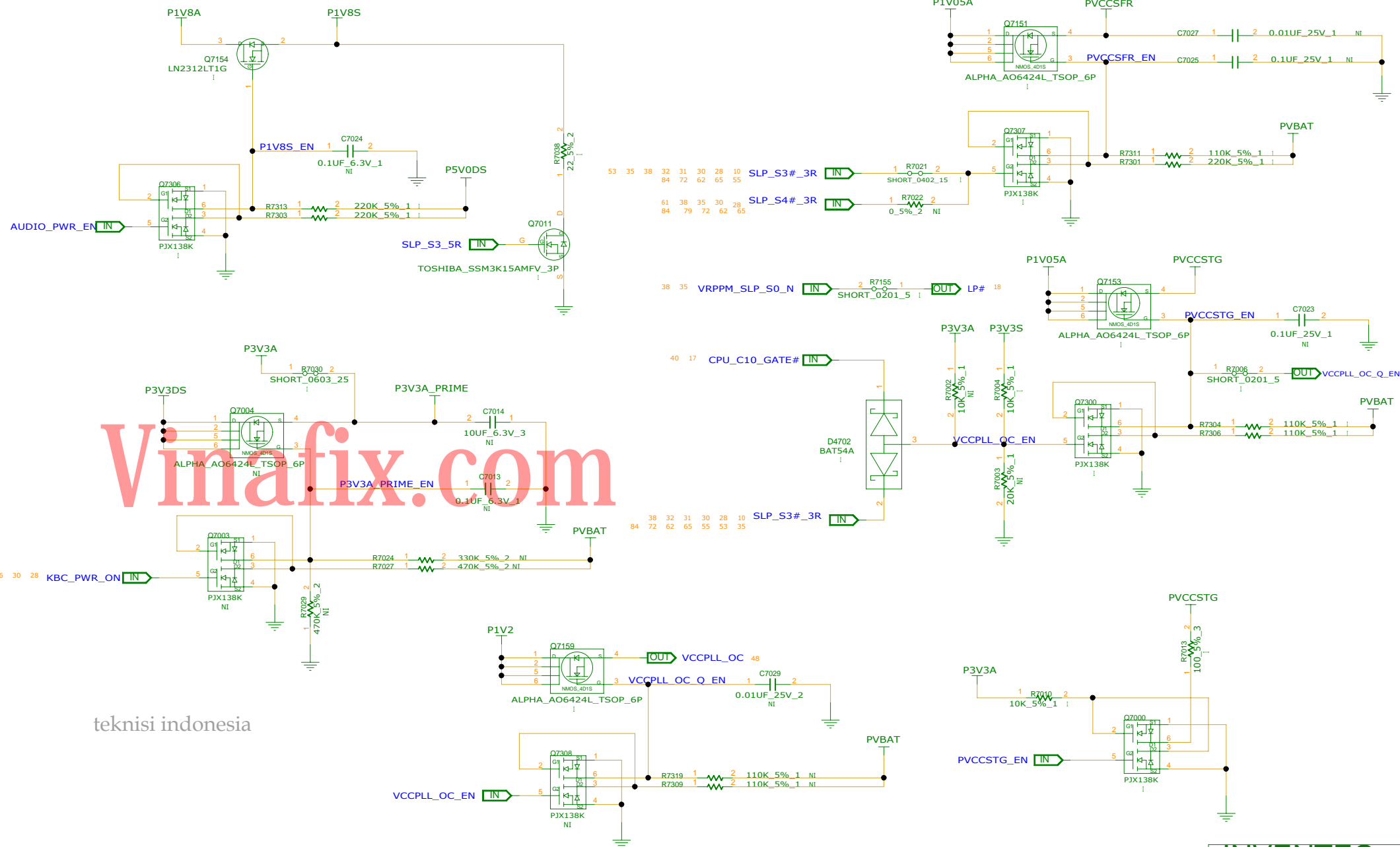
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MODEL PROJECT FUNCTION
POWER SEQUENCE (P3V3S,P5V0S)SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01
SHEET 30 of 105CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxx PCB VER XXX

D

C

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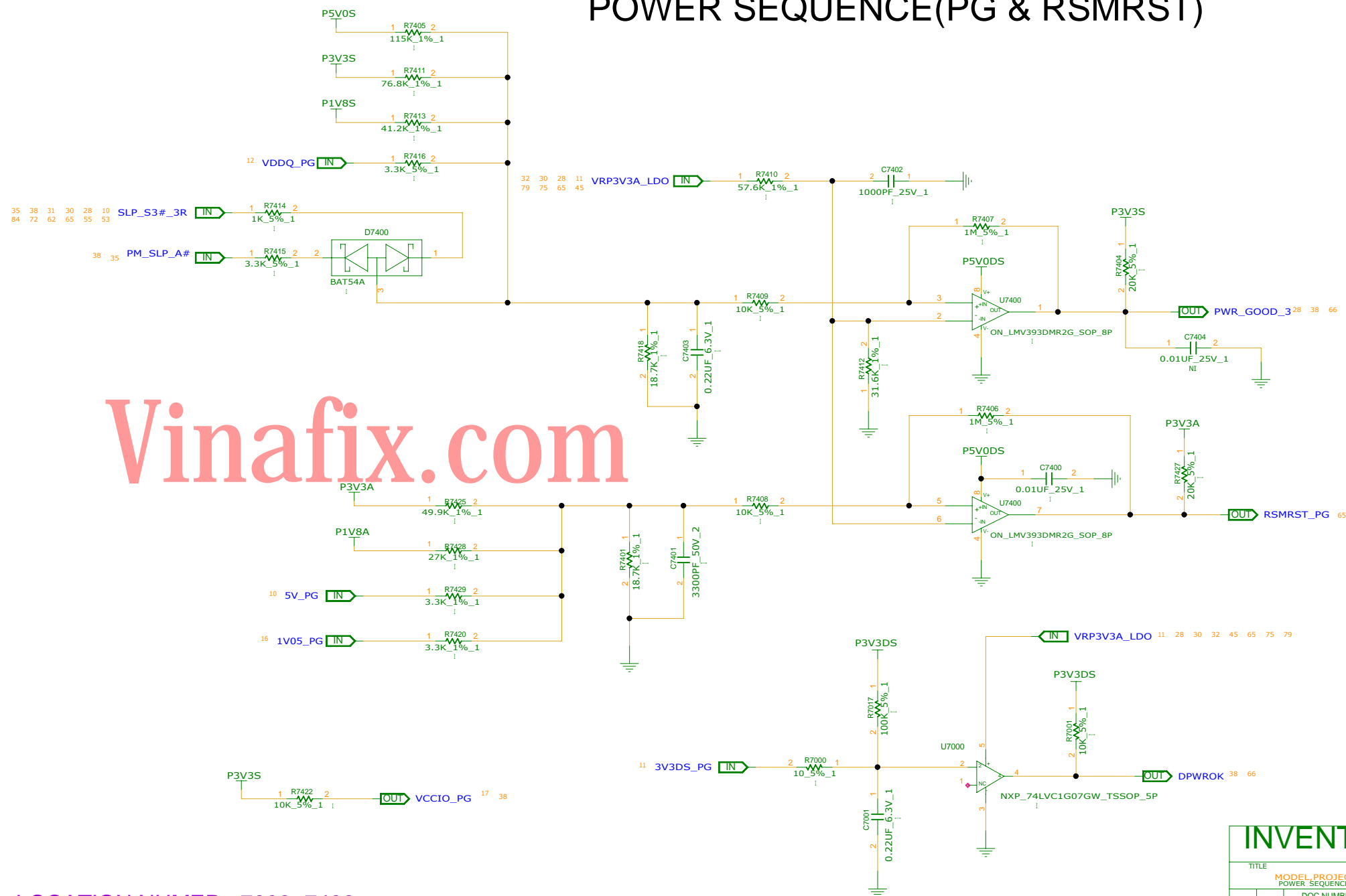
LOCATION NUMER : 7000~7499

POWER SEQUENCE(P1V8,PCH POWER)

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
POWER SEQUENCE(P1V8,PCH POWER)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 31 of 105			

POWER SEQUENCE(PG & RSMRST)



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LOCATION NUMER : 7000~7499

INVENTEC

TITLE
MODEL PROJECT FUNCTION
POWER SEQUENCE(PG & RSMRST)

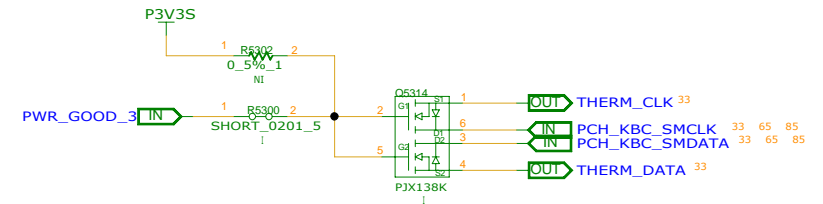
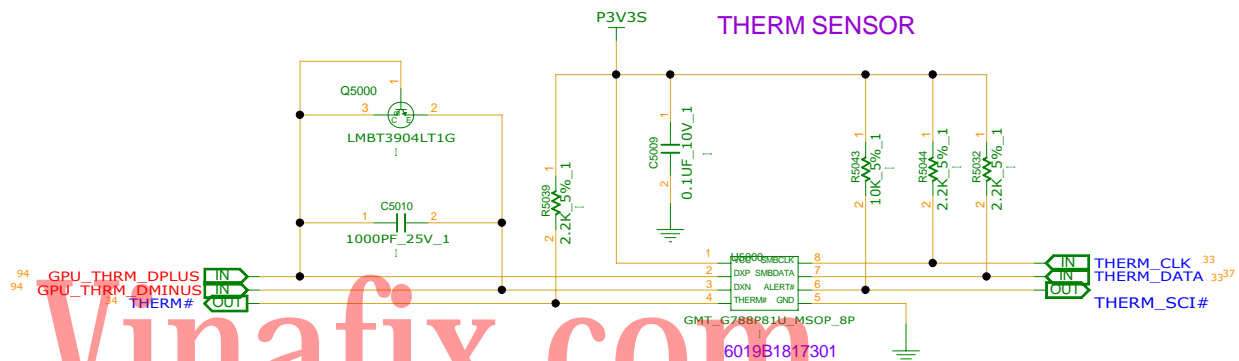
SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

SHEET 32 of 105

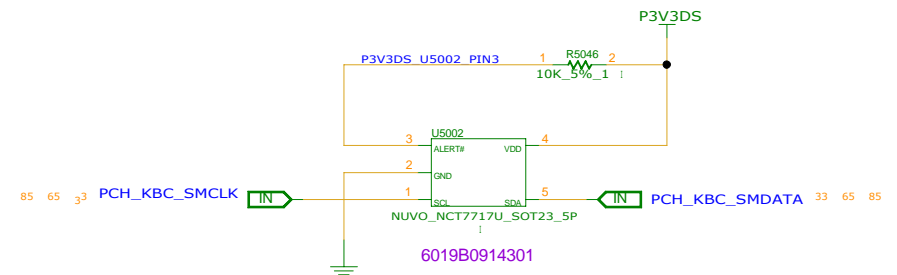
CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx PCB VER XXX

THERMAL

REFERENCE NUMBER:4400~5400



DIS AMBIENT TEMP SENSOR MOVE TO POWER BUTTON BOARD PAGE97



LOCATION NUMBER:4411~4449

INVENTECTITLE
MODEL,PROJECT,FUNCTION

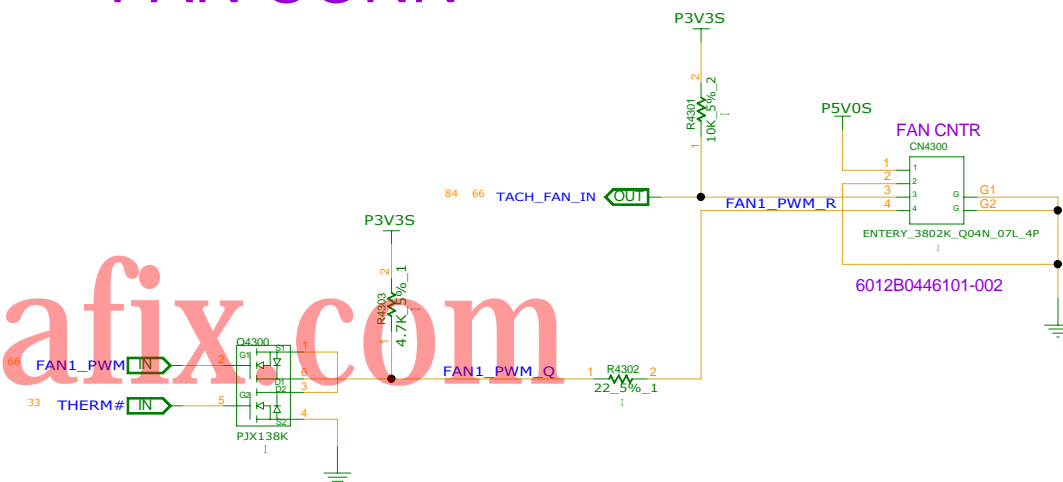
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by	DATE
XXX	21-OCT-2002

PCB P/N 60xxxxxxxxxxx

PCB VER XXX

SHEET 33 of 105



LOCATION NUMBER:4300~4349

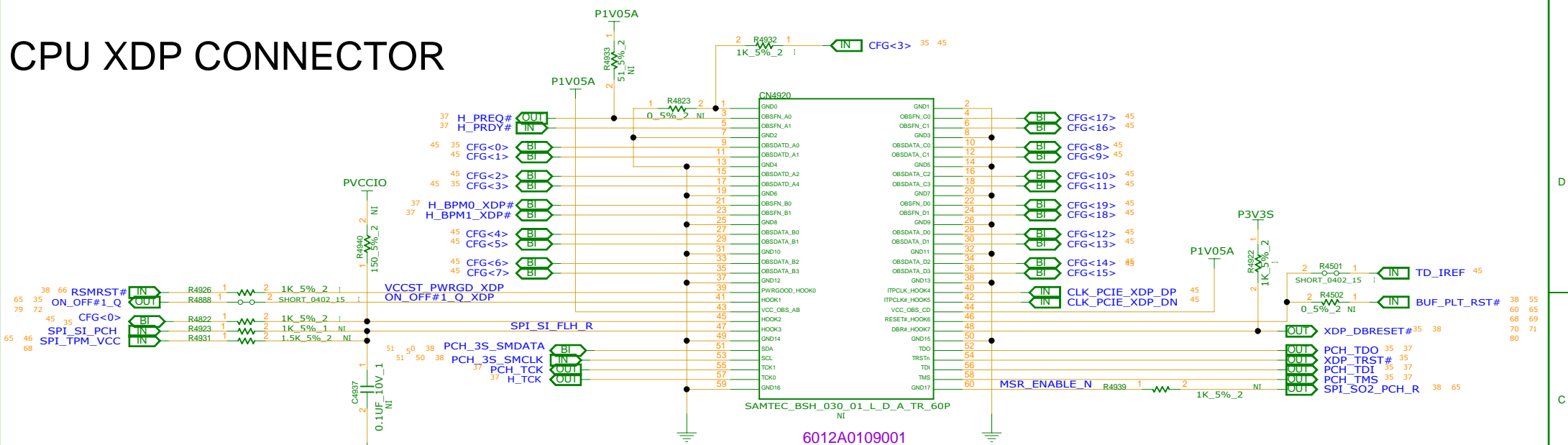
CHANGE by		XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx		PCB VER	XXX	SHEET 34 of 105			

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION	FAN CNTR
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20	20	20
21	21	21
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25	25	25
26	26	26
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99	99	99
100	100	100

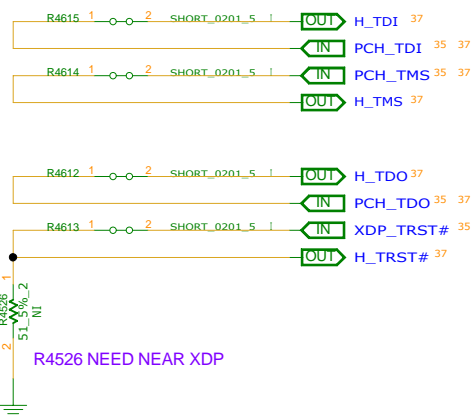
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET		34 of 105	

CPU XDP CONNECTOR



C4937 NEED NEAR XDP

Vinafix.com



R4526 NEED NEAR XDP

FOR ME TEST
NEED TO BE PLACE BETWEEN
KEYBOARD OR BOTTOM DOOR

6012B0622401-002

LOCATION NUMBER:4500~4999

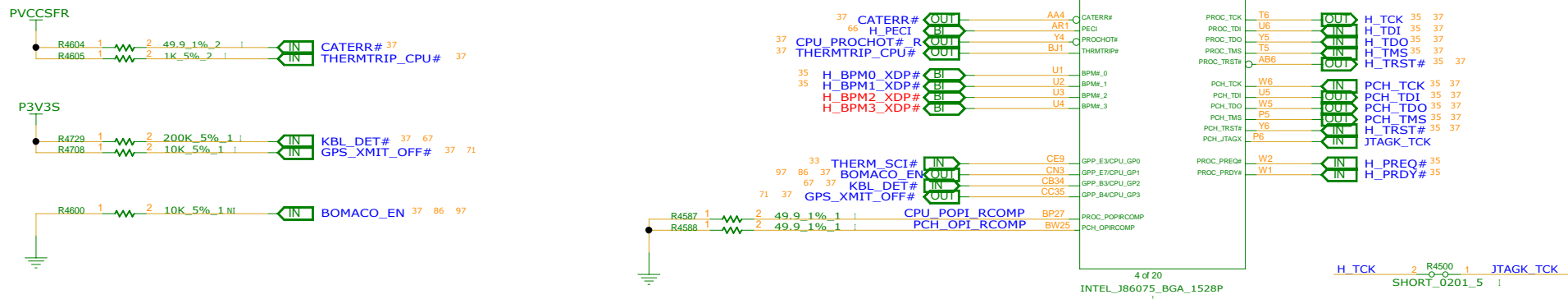
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION	REV	X01
SIZE	A3	CODE	CS
SHEET	35 of 105	DOC NUMBER	1310xxxxx-0-0

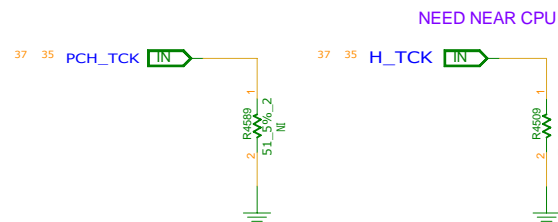
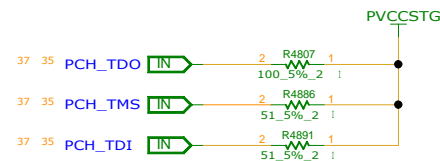
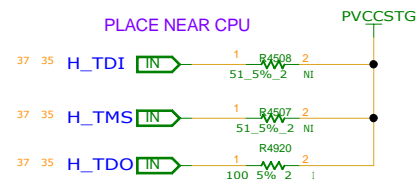
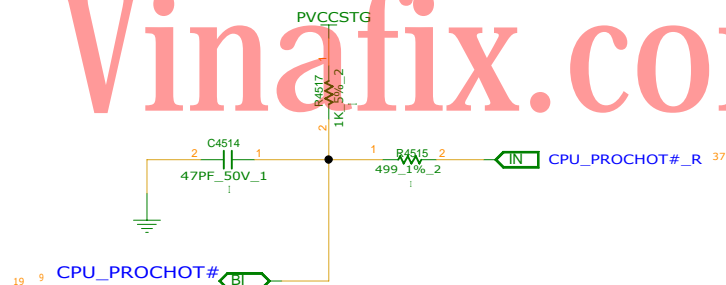


CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



LAYOUT NOTE: PLACE R4808 NEAR PCH
LAYOUT NOTE: JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP

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LOCATION NUMBER: 4500~4999

INVENTEC

TITLE
MODEL PROJECT, FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 37 of 105





D

C

B

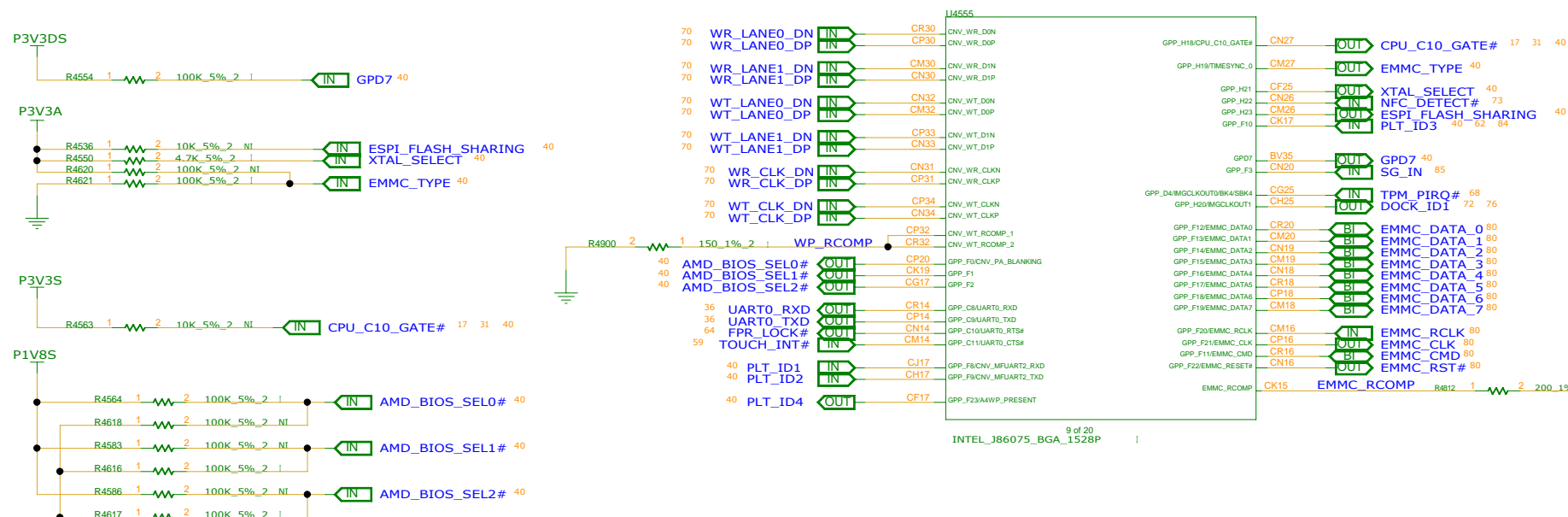
A

D

C

B

A



INTEL_J86075_BGA_1528P

PLT_ID1	PLT_ID2	PLT_ID3	PLT_ID4	ALS_DETECT#	
0	1	0	X	X	CRESCENT 14" VPRO
0	1	1	X	X	CRESCENT 15" VPRO
1	1	0	X	X	CRESCENT 14" NON-VPRO
1	1	1	X	X	CRESCENT 15" NON-VPRO
			X	1	CRESCENT NON-ALS
			X	0	CRESCENT HAVE ALS
			0	X	CRESCENT NON-EMMC
			1	X	CRESCENT HAVE EMMC

NOTE : DEFAULT MB IS DIS , W SERIES , 15" , VPRO , NON-ALS SKU , HAVE EMMC SKU

LOCATION NUMBER:4500~4999

INVENTEC

TITLE
MODEL PROJECT FUNCTION
MCP4-GPIO & CNV1SIZE A3
CODE CS
DOC NUMBER 1310xxxx-0-0
REV X01
SHEET 40 of 105CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

D

C

B

A

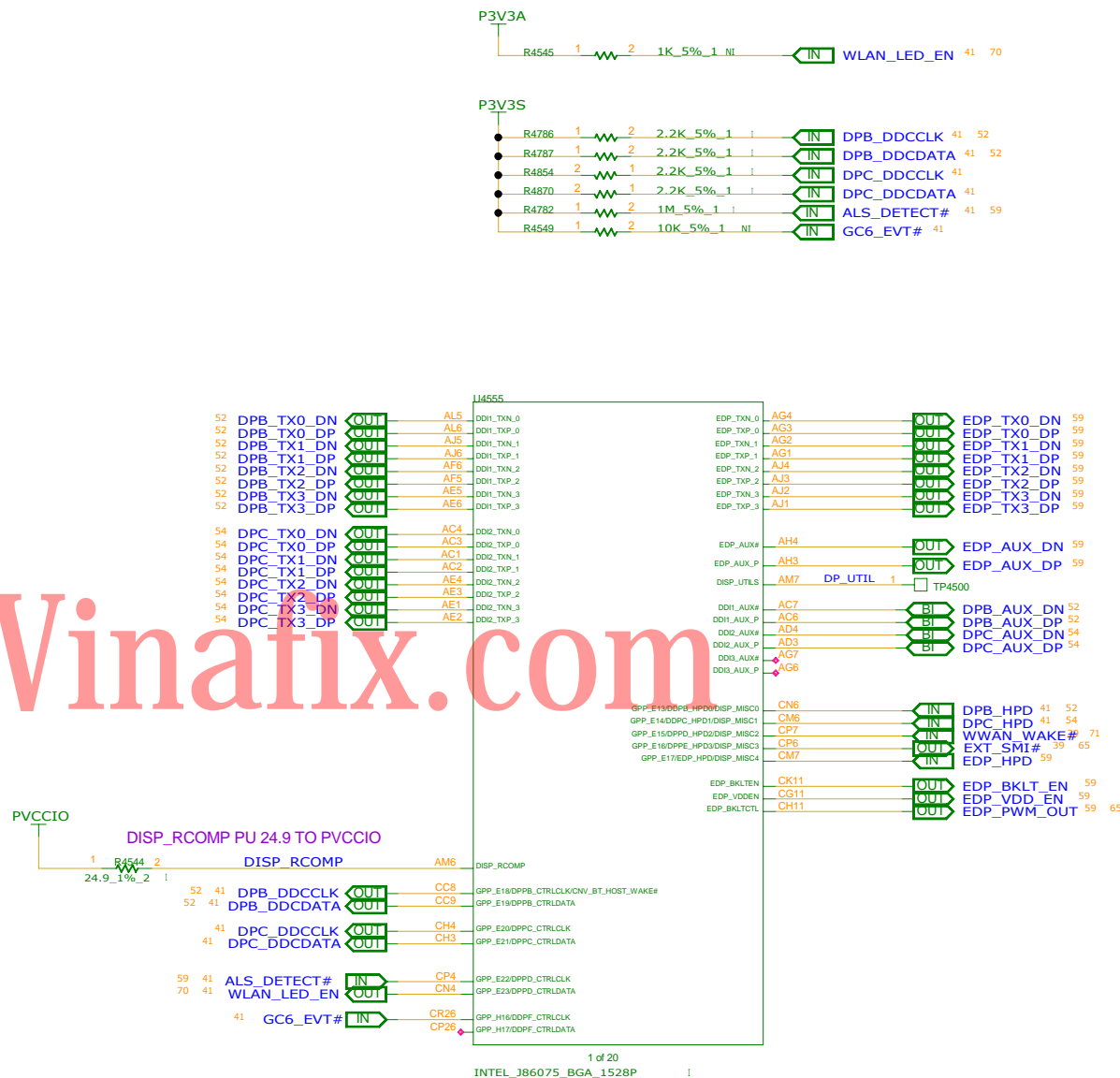
D

C

B

A

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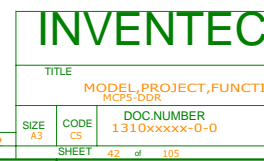


LOCATION NUMBER:4500~4999

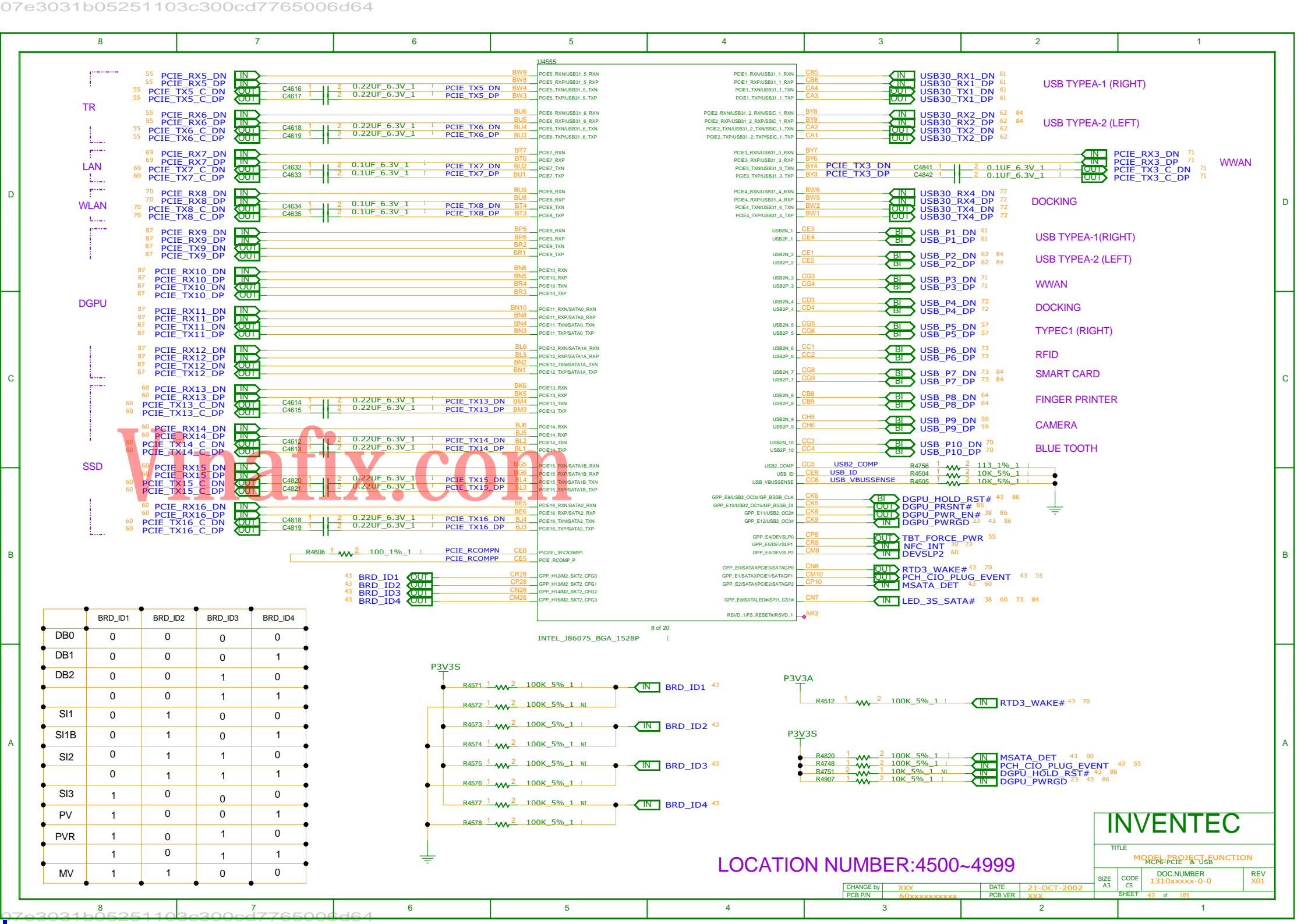
INVENTEC

TITLE
MODEL PROJECT FUNCTION
MCP4-GPIO & DPSIZE A3
CODE CS
DOC NUMBER 1310xxxxx-0-0
REV X01

SHEET 41 of 105



	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
	SHEET		42 of 105



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION MCP7-RTC & AUDIO & SATA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 44 of 105			

D

C

B

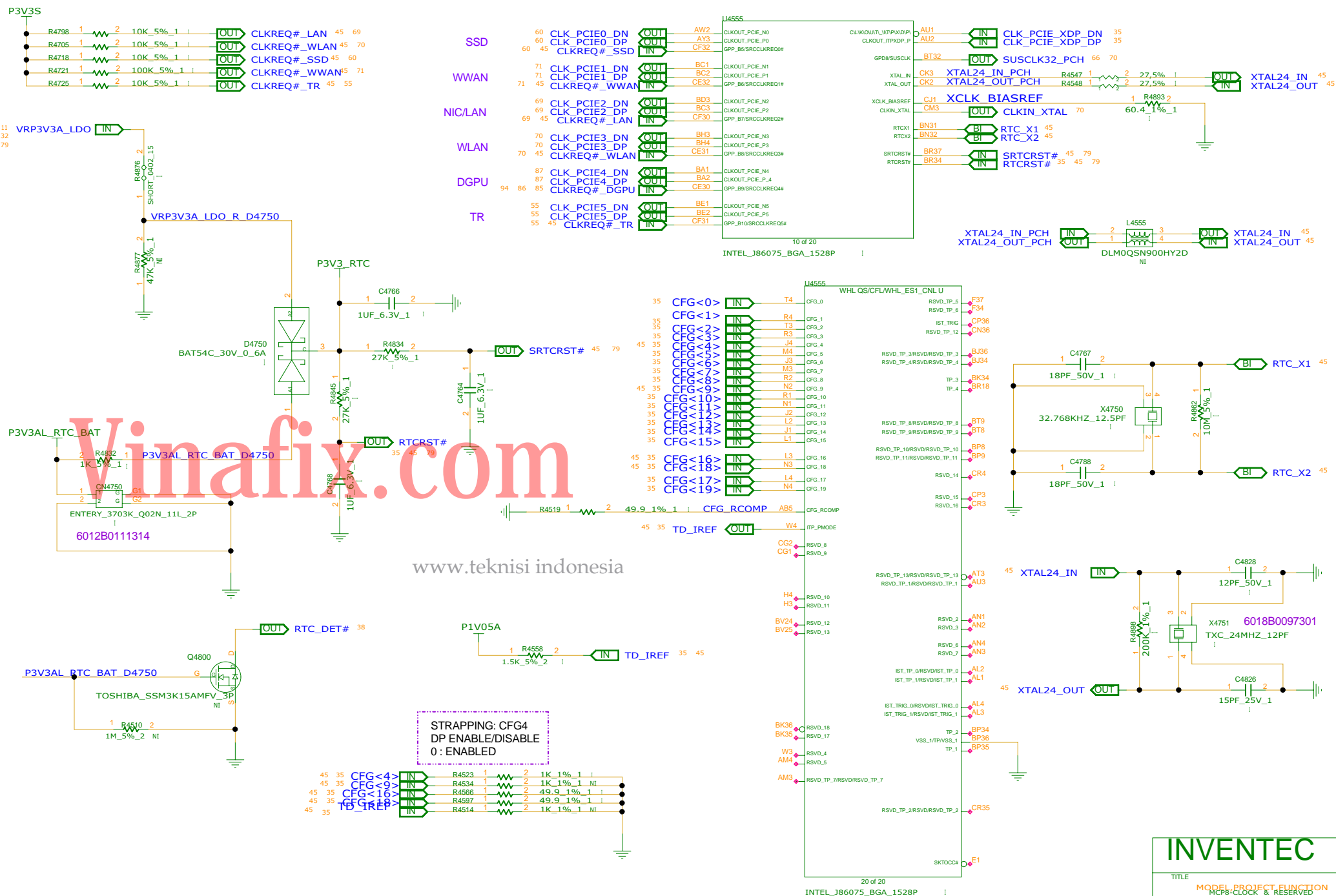
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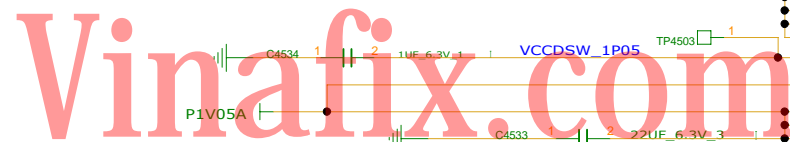
D

C

B

A





INTEL J86075 BGA 1528P

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

D

C

B

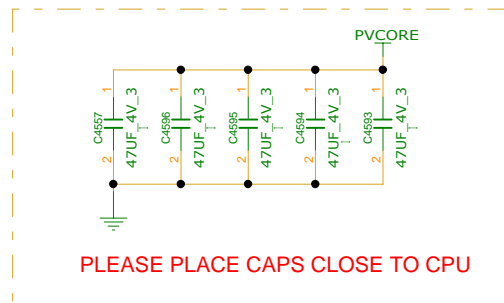
A

D

C

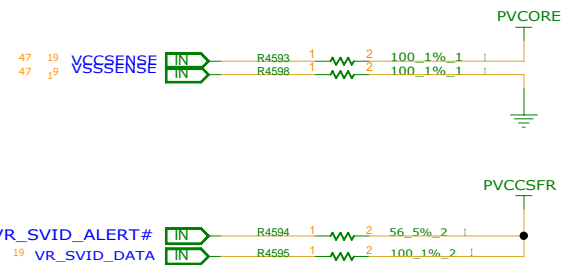
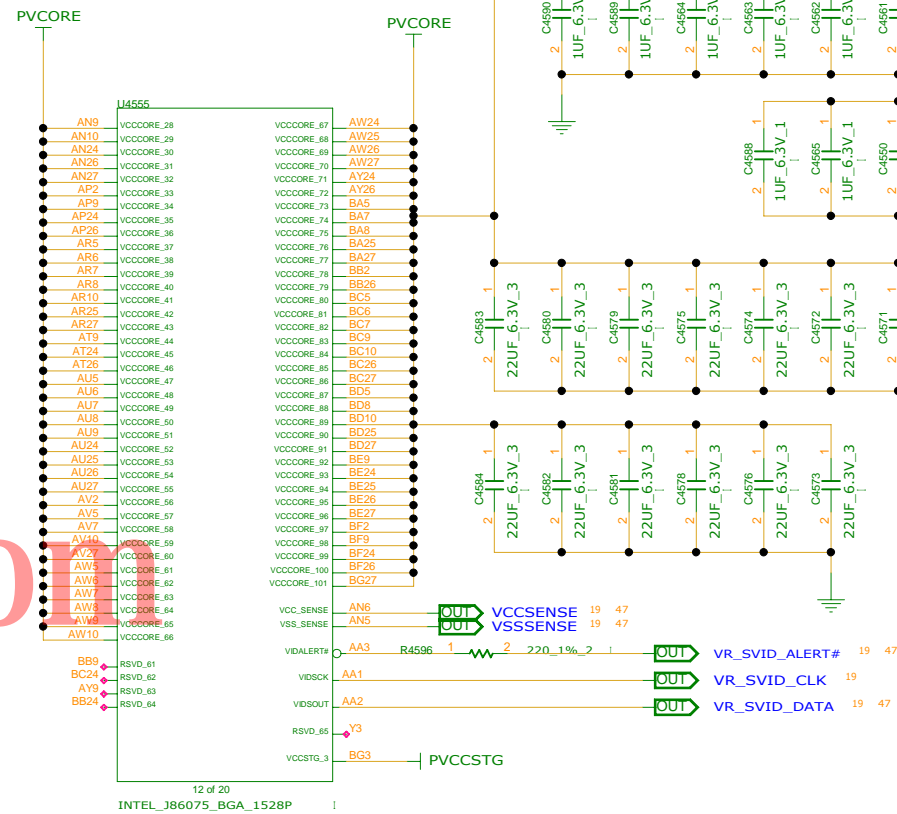
B

A



PLEASE PLACE CAPS UNDER CPU

Vinafix.com



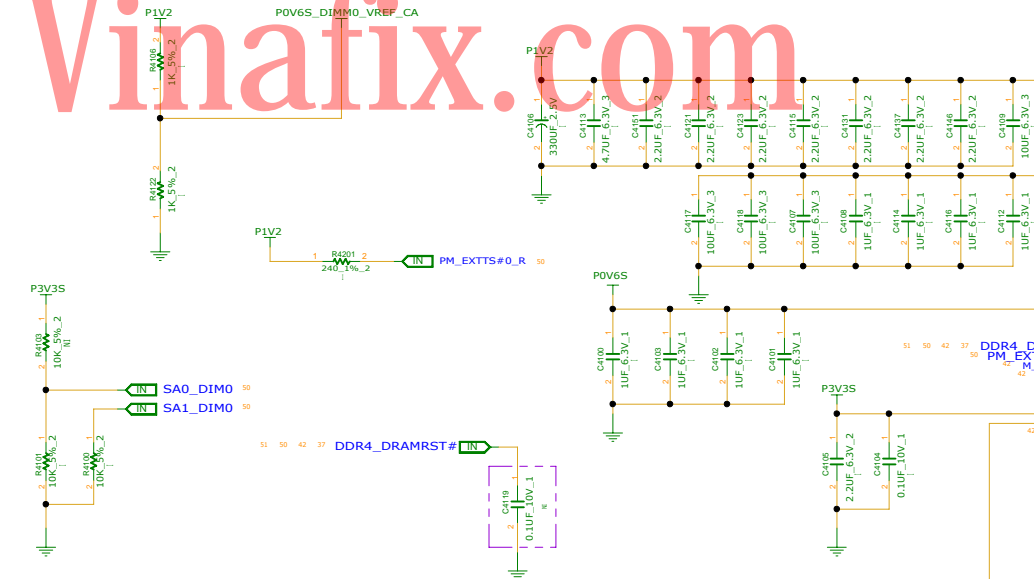
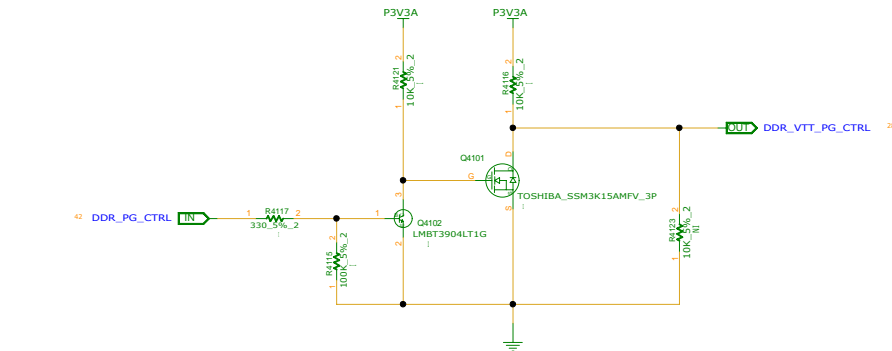
LOCATION NUMBER:4500~4999

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC			
TITLE MODEL PROJECT,FUNCTION RCPT0-POWER1			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		47 of 105	

DDR4 DIMM0

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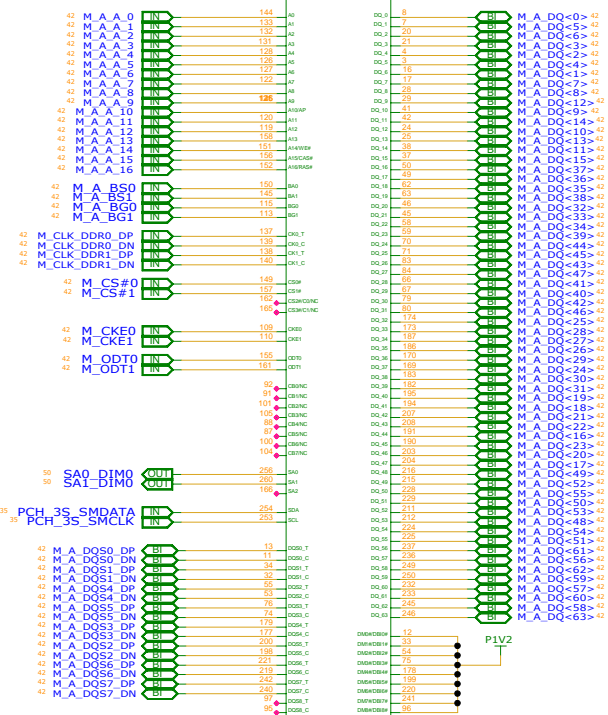


NOTE:
IF SA0_DIM0=0, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

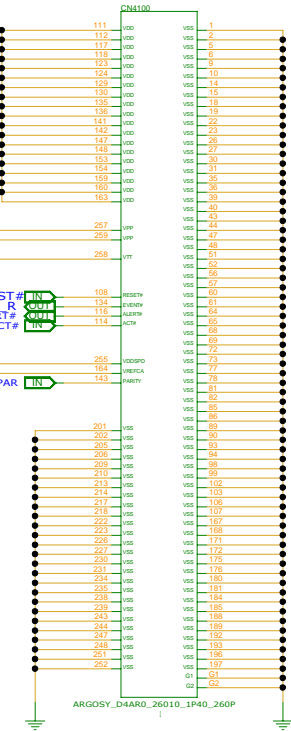
IF SA0_DIM0=1, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

PLACE C4119 WITHIN 200 MILS
FROM THE SODIMM - 0 (CN4100)

LOCATION NUMBER:4100~4299



ARGOSY_D4ARO_26010_IP40_260P
6026B0328101-004

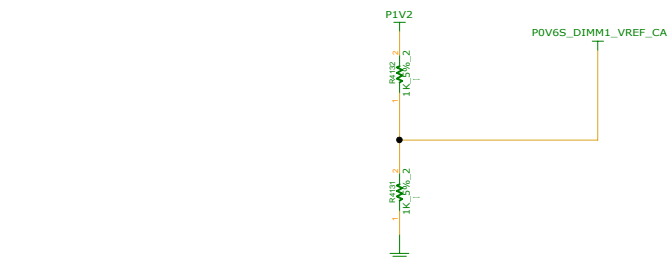


INVENTEC

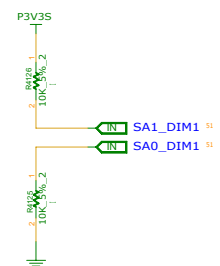
MODEL PROJECT FUNCTION
DDR4 SO-DIMM0

CHANGE H	XXX	DATE	21-OCT-2002	DOC NUMBER	REV
PCB PIN	PCB VER	SHEET	50	1	

DDR4 DIMM1

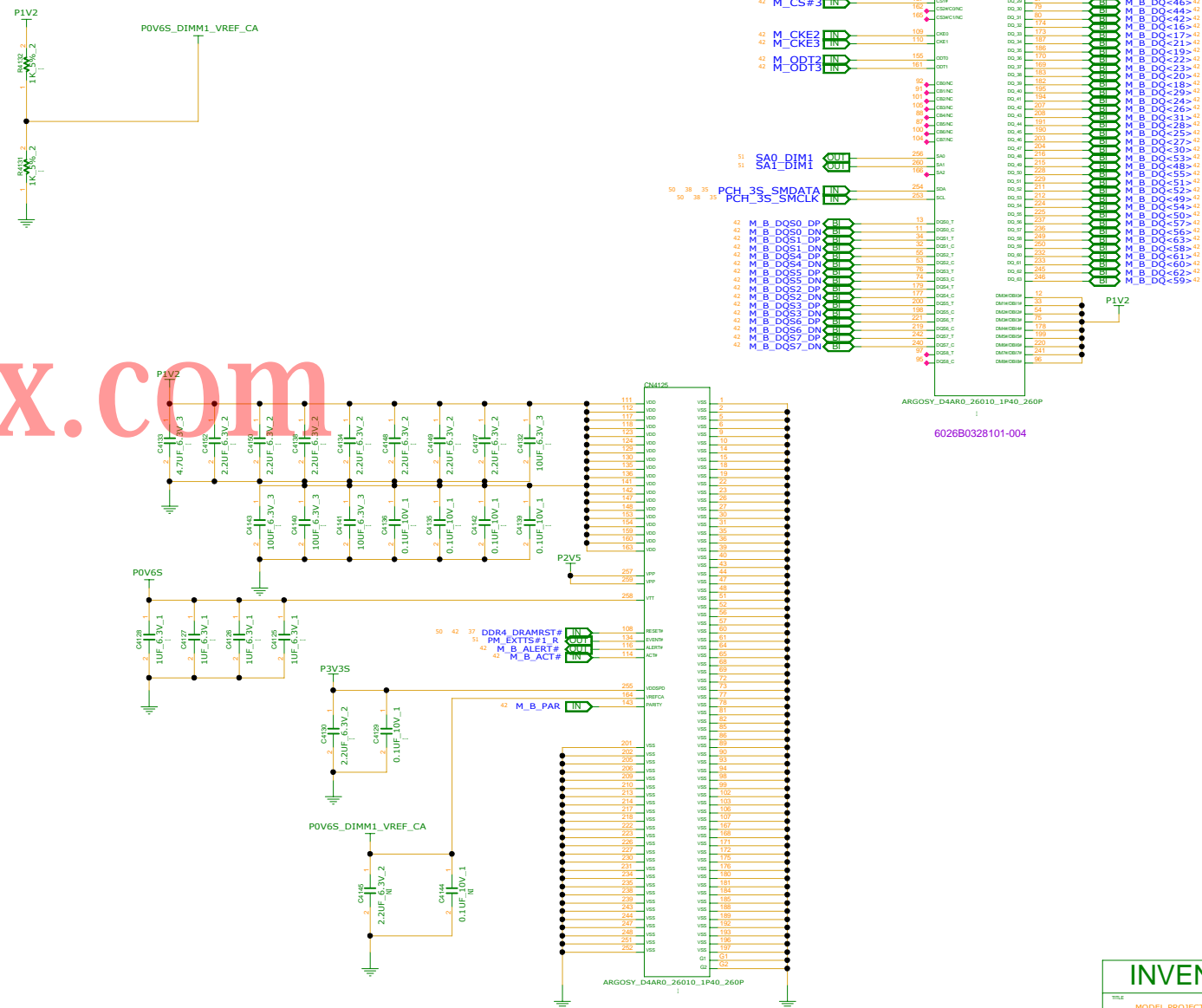


The logo for winatix.com is displayed in a large, red, serif font. Below the logo, a horizontal timeline is shown with a yellow background. The timeline has a vertical axis on the left labeled 'P1V2' with a downward arrow. The timeline itself is marked with several points labeled 'W.2' and 'W.3' in black text. The points are connected by a series of horizontal and vertical lines, forming a step-like pattern. The timeline ends with a small black dot.



NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34

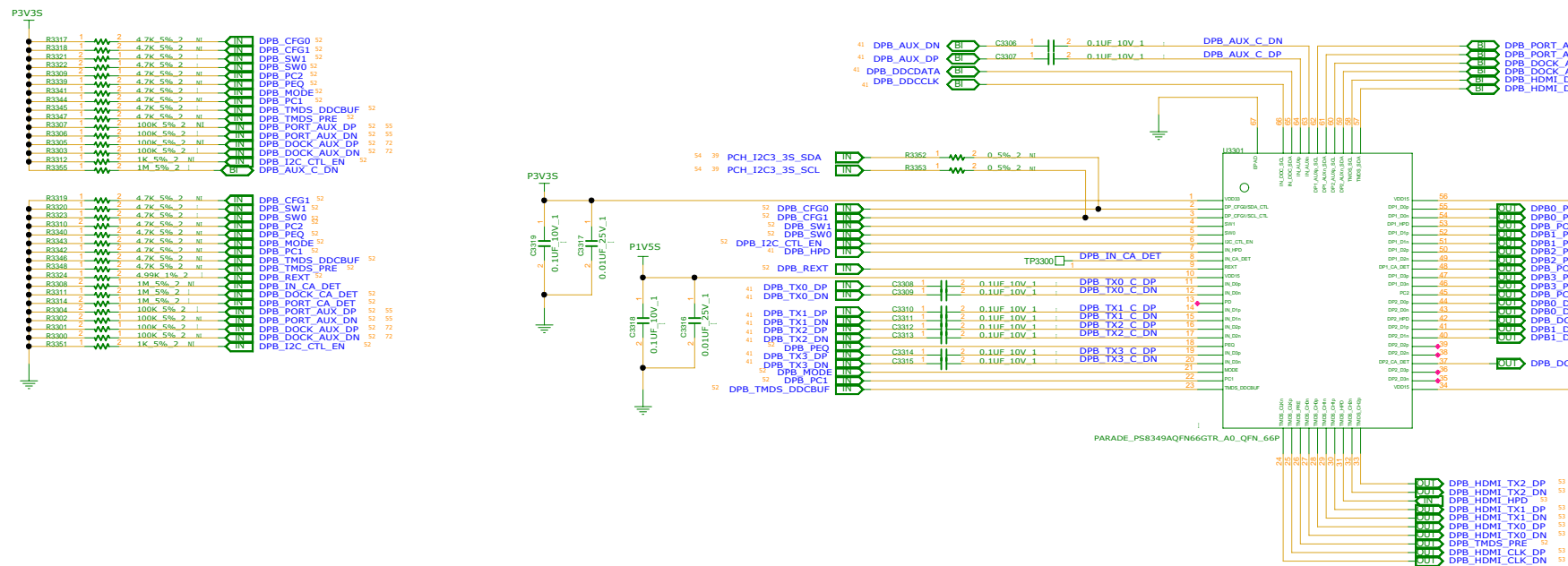
LOCATION NUMBER:4100~4299



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION DDR4 SO-DIMM1			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 51 of 105			

CHANGE BY	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB PIN	60xxxxxxxxxx	PCB VER	XXX	SHEET		51	of	105			



4-LANE DP1.2 DEMUX
TMD5 : HDMI , PRIORITY2
DP1 : TR , PRIORITY3
DP2 : DOCKING(VGA) , PRIORITY1
AUTO AWITCH MODE

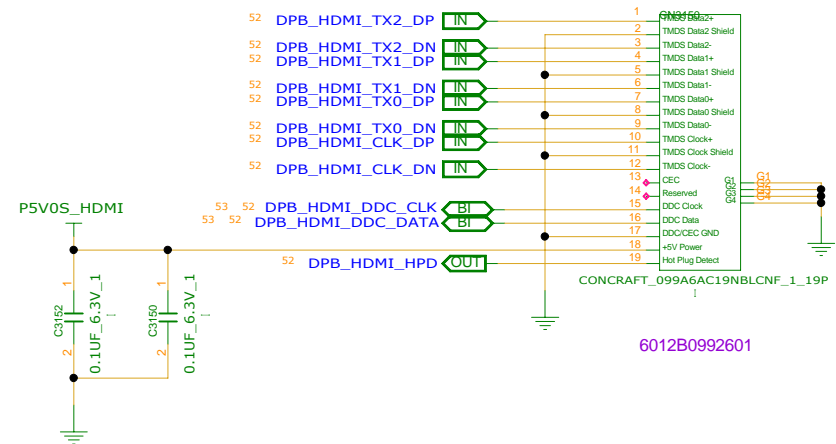
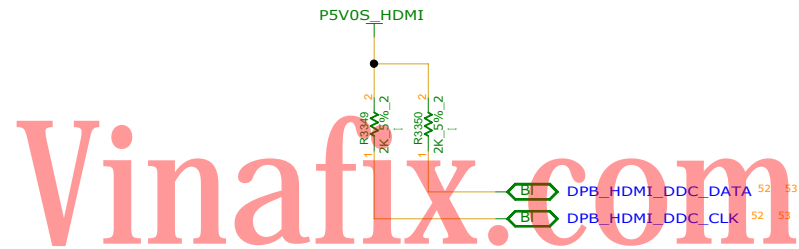
LOCATION NUMBER:3300-3399

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
DPB TO DP DEMUX(P58349A)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310VXXXX-0-0	201
SHEET		#	USE

CHNGEN	XXX	DATE	21-OCT-2002
PCB PIN	66XXXXXXXXXX	PCB VER	XXX

The schematic diagram illustrates the P5V0S power supply regulation circuit. It features a 5V regulator (U3150) with its input connected to P5V0DS, its output connected to P5V0S_HDMI, and its enable pin connected to SLP_S3#_3R. The regulator is powered by a 1uF capacitor (C3151) connected to ground. The output is also connected to a 1uF capacitor (C3151) connected to ground. The output voltage is 6.3V.



INVENTEC

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 53 of 105			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

D

C

B

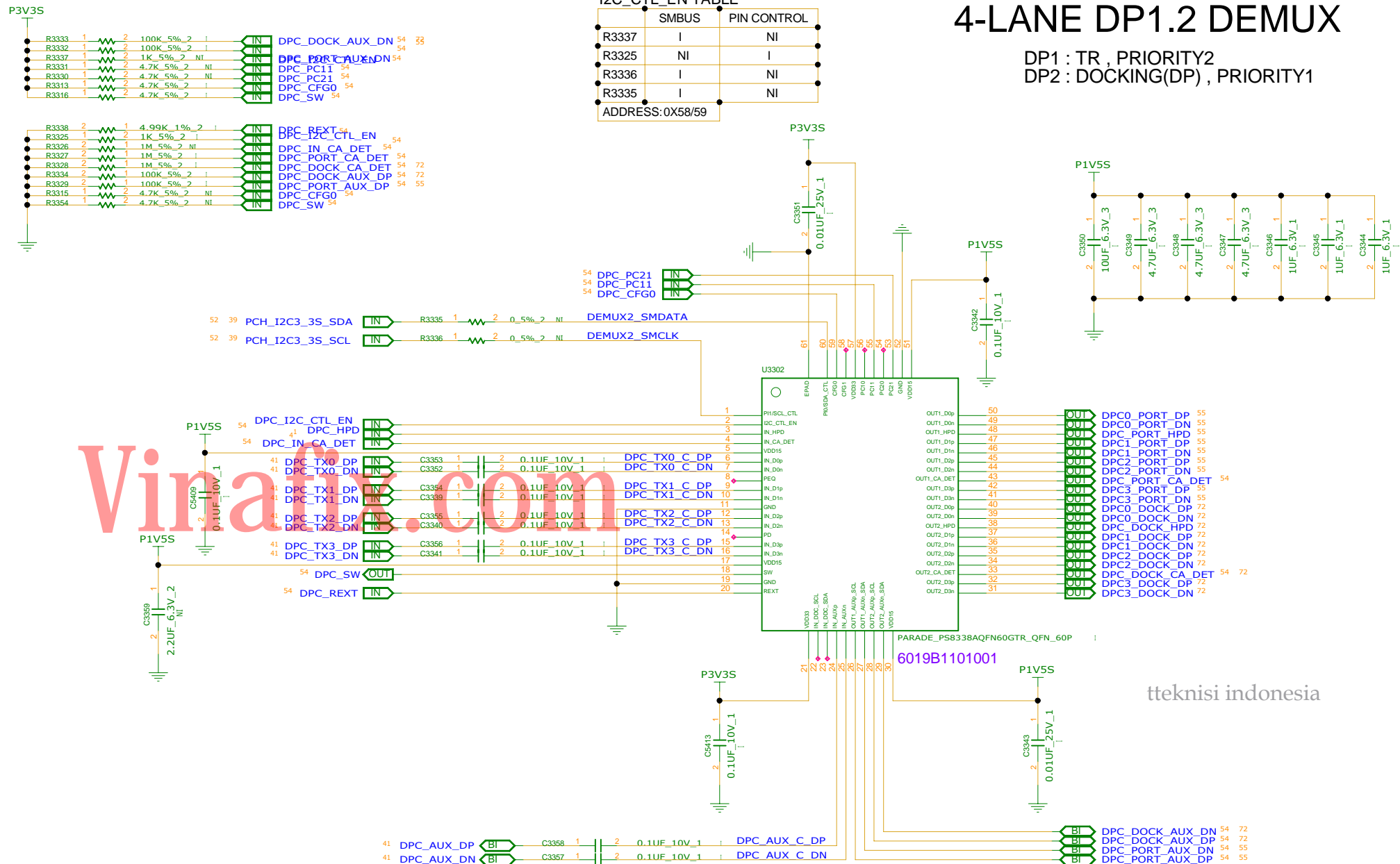
A

I2C_CTL_EN TABLE

	SMBUS	PIN CONTROL
R3337	I	NI
R3325	NI	I
R3336	I	NI
R3335	I	NI
ADDRESS:0X58/59		

4-LANE DP1.2 DEMUX

DP1 : TR , PRIORITY2
DP2 : DOCKING(DP) , PRIORITY1



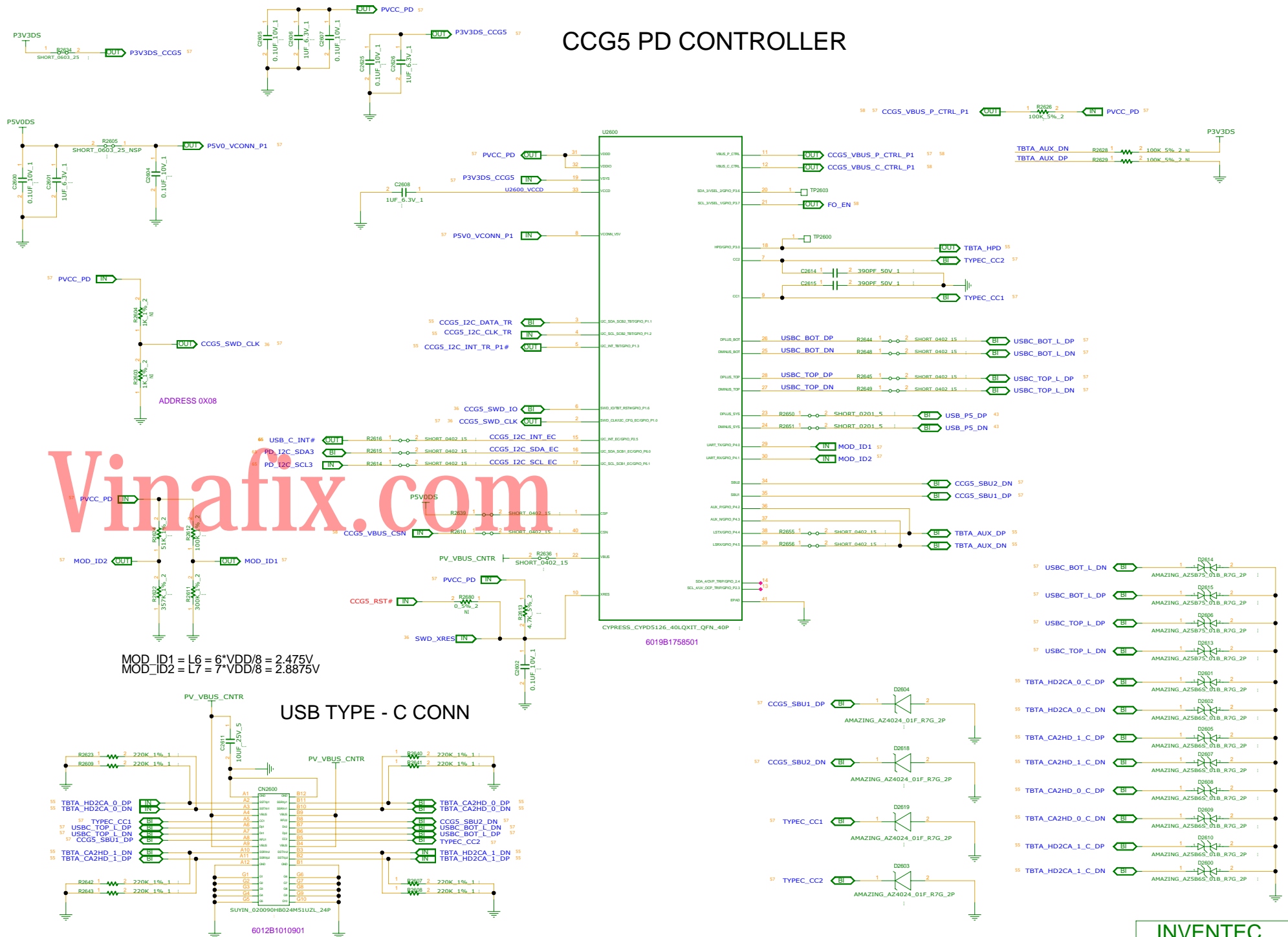
LOCATION NUMBER:3300~3399





GND

CCG5 PD CONTROLLER

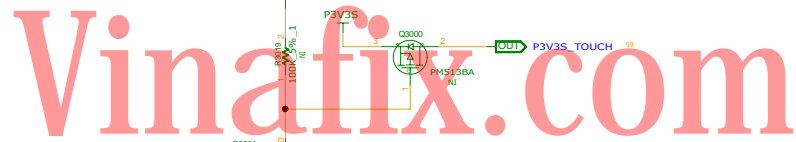


INVENTEC			
MODEL,PROJECT,FUNCTION			
USB_TYPEC_1			
CHGEMEN	XXX	DATE	21-OCT-2002
PCB PIN	6012B1010901	PCB VER	XXX
SIZE	CS	DOC NUMBER	131010XXXX-0-10
C	SHEET	57	REV
1			

LOW VOLTAGE PATH



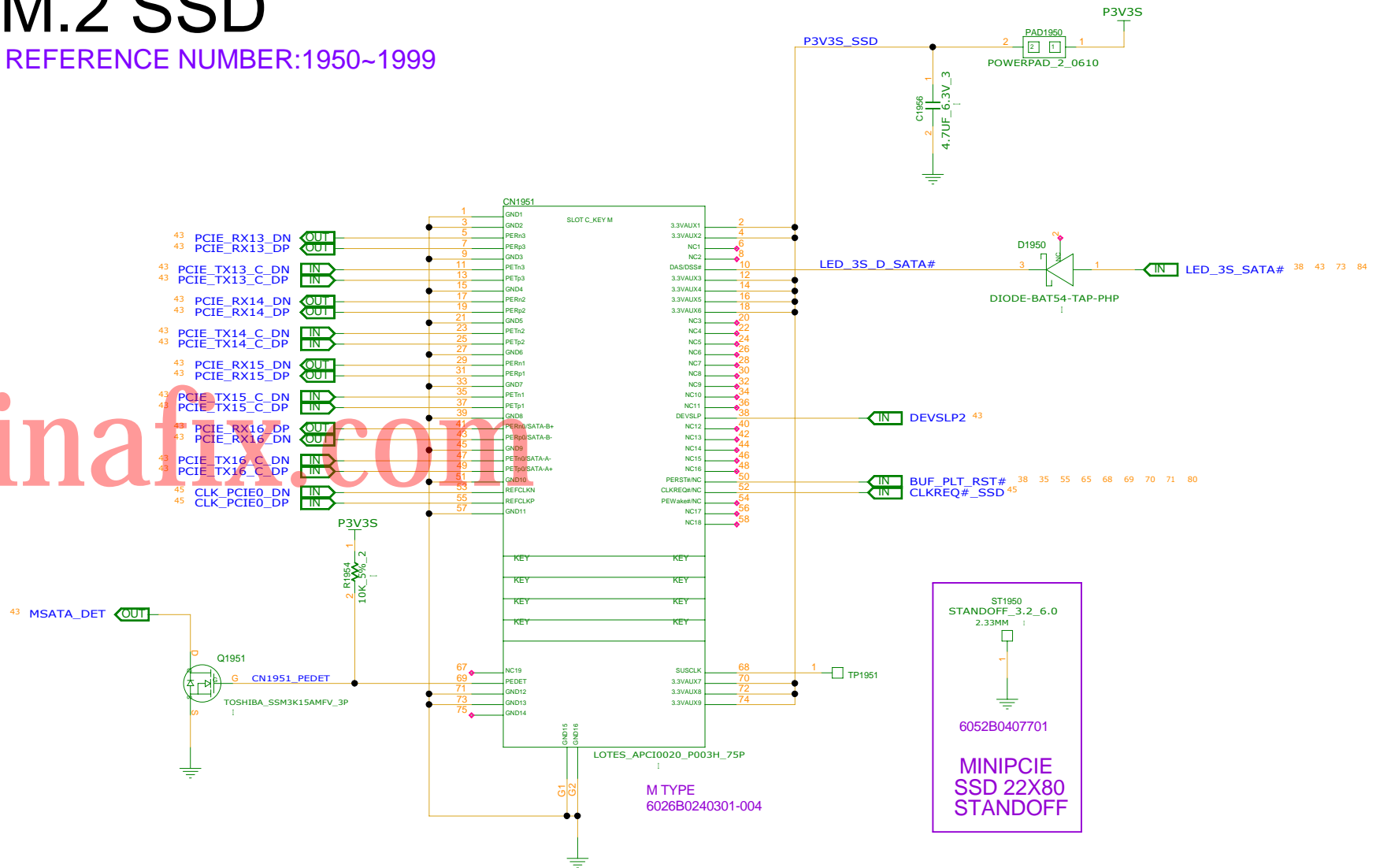
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX



M.2 SSD

REFERENCE NUMBER:1950~1999

Vinafix.com



LOCATION NUMBER:1950~1999

INVENTECTITLE
MODEL,PROJECT,FUNCTION

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

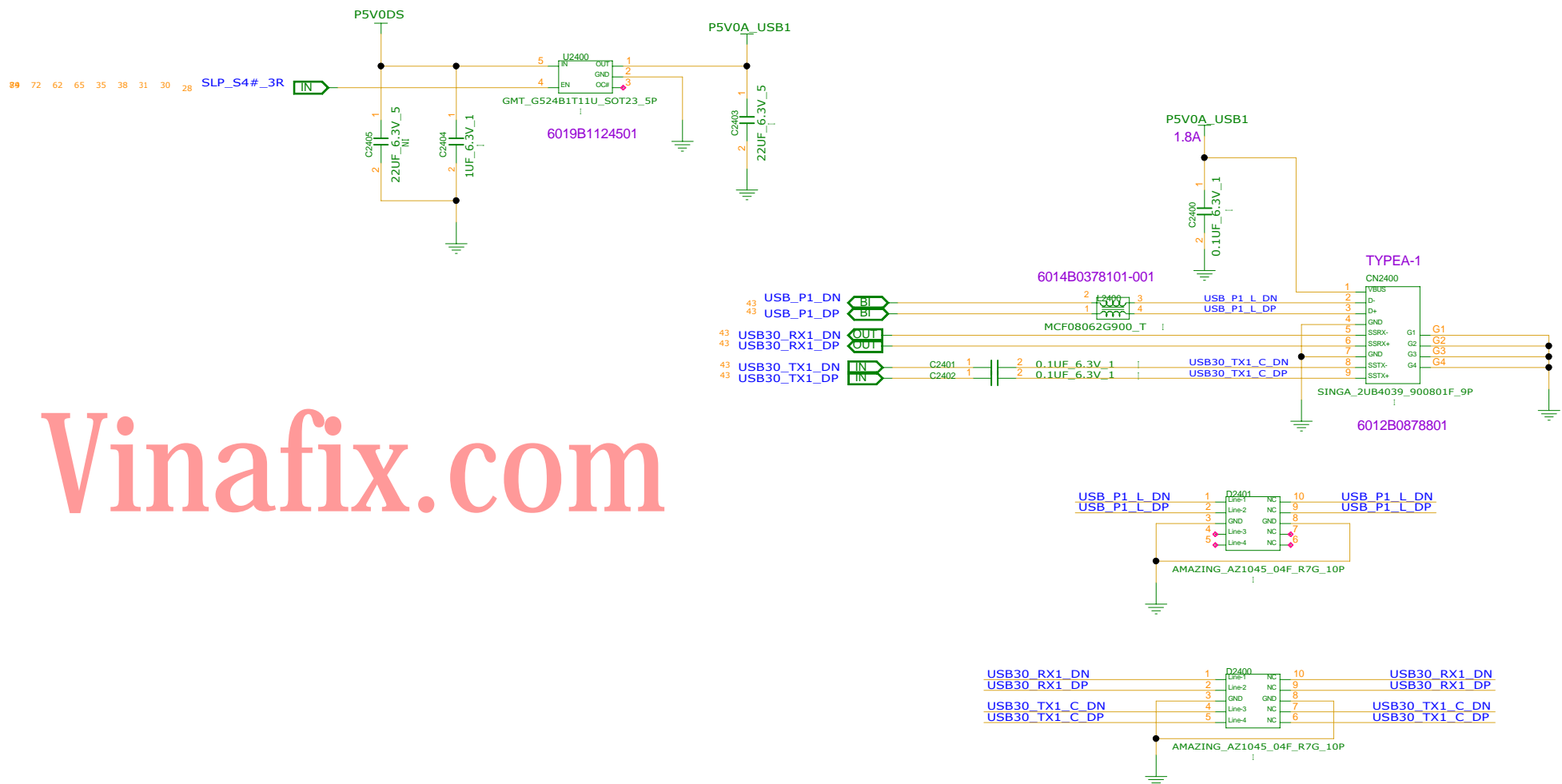
CHANGE by	DATE
XXX	21-OCT-2002

PCB P/N	PCB VER
60xxxxxxxxxx	XXX

SHEET 60 of 105

M/B USB3.0 (RIGHT)

REFERENCE NUMBER:2400~2500



Vinafix.com

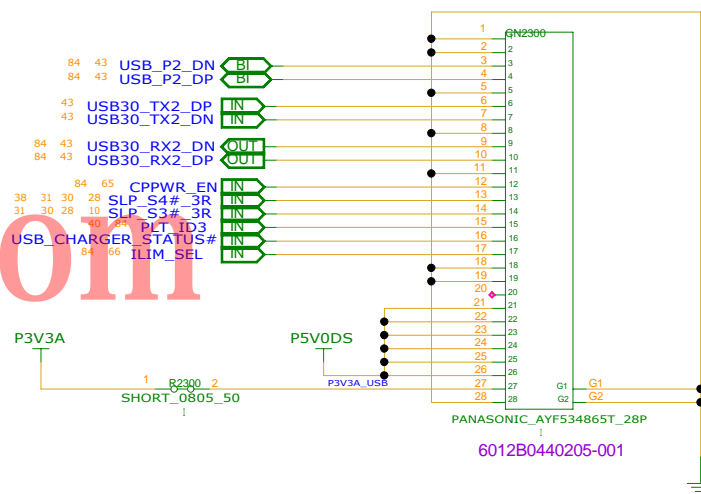
LOCATION NUMBER:2400~2499

INVENTECTITLE
MODEL PROJECT,FUNCTION

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		61 of 105	

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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M/B TO USB/B CNTR

www.teknisi-indonesia.com

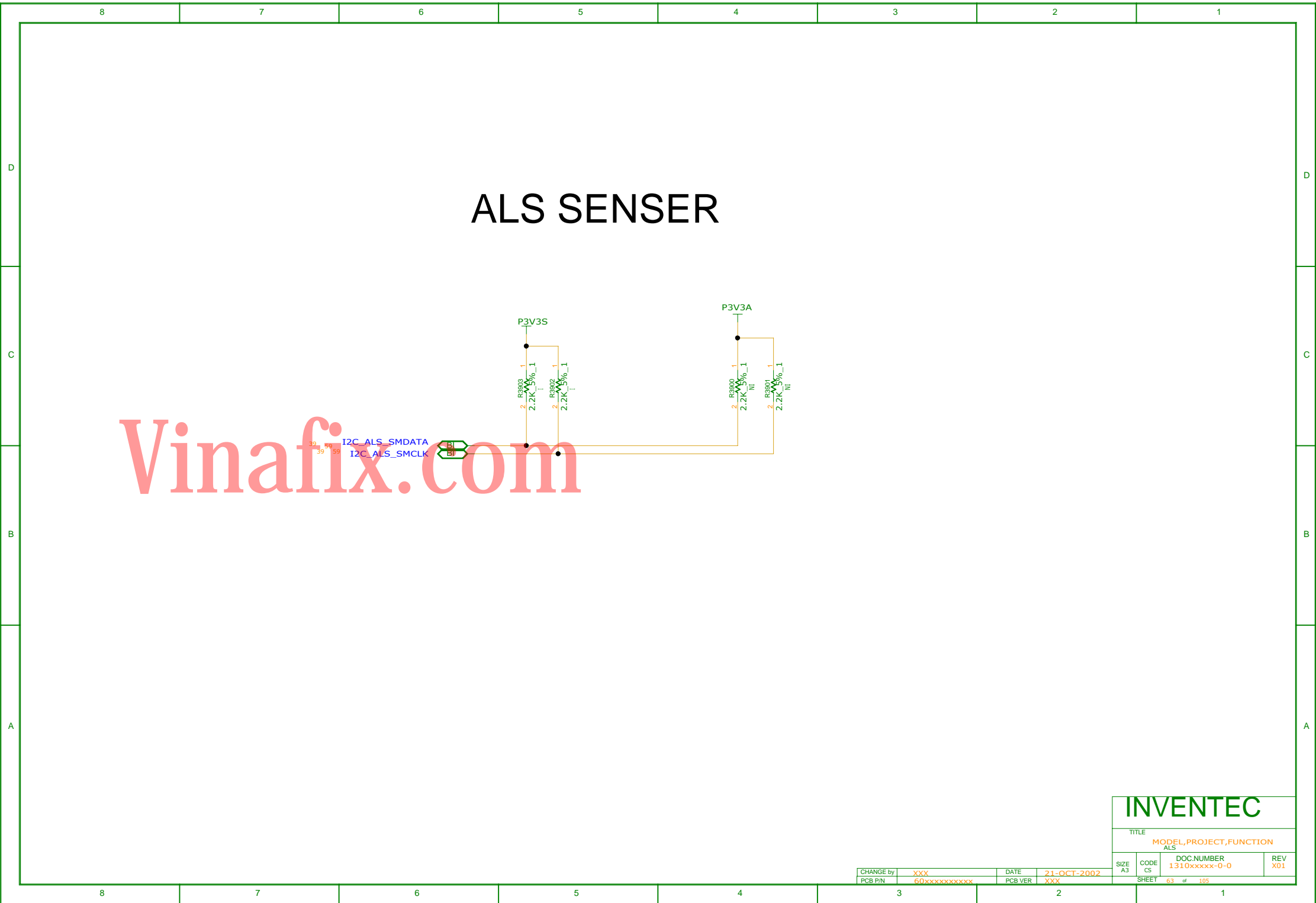
LOCATION NUMBER:2500~2599

INVENTEC

TITLE
MODEL PROJECT,FUNCTION
USB_DB_CONN

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		62 of 105	

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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ALS SENSER

Vinafix.com

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
ALS			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 63 of 105			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

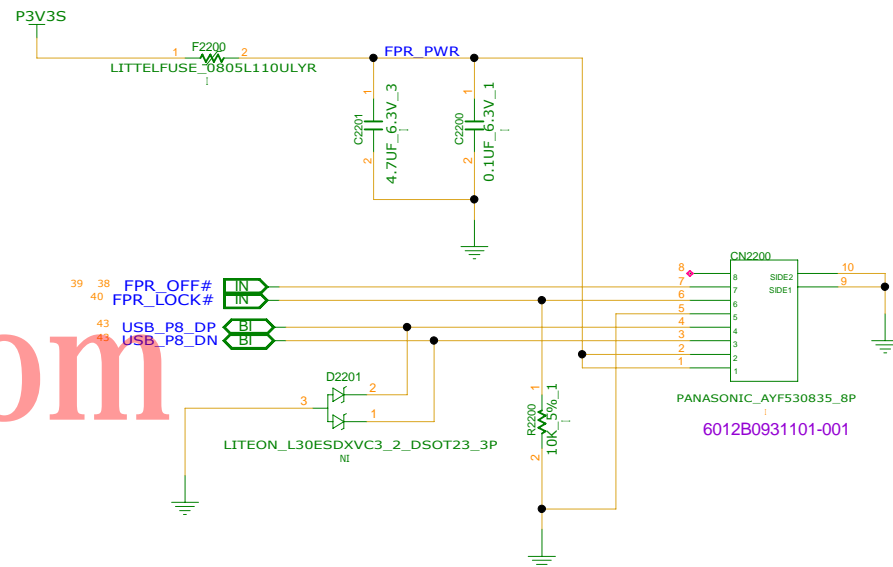
D

C

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A

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FINGER PRINT CONN

LOCATION NUMBER:2200~2249

INVENTEC

TITLE
MODEL PROJECT,FUNCTION
FINGER PRINTER

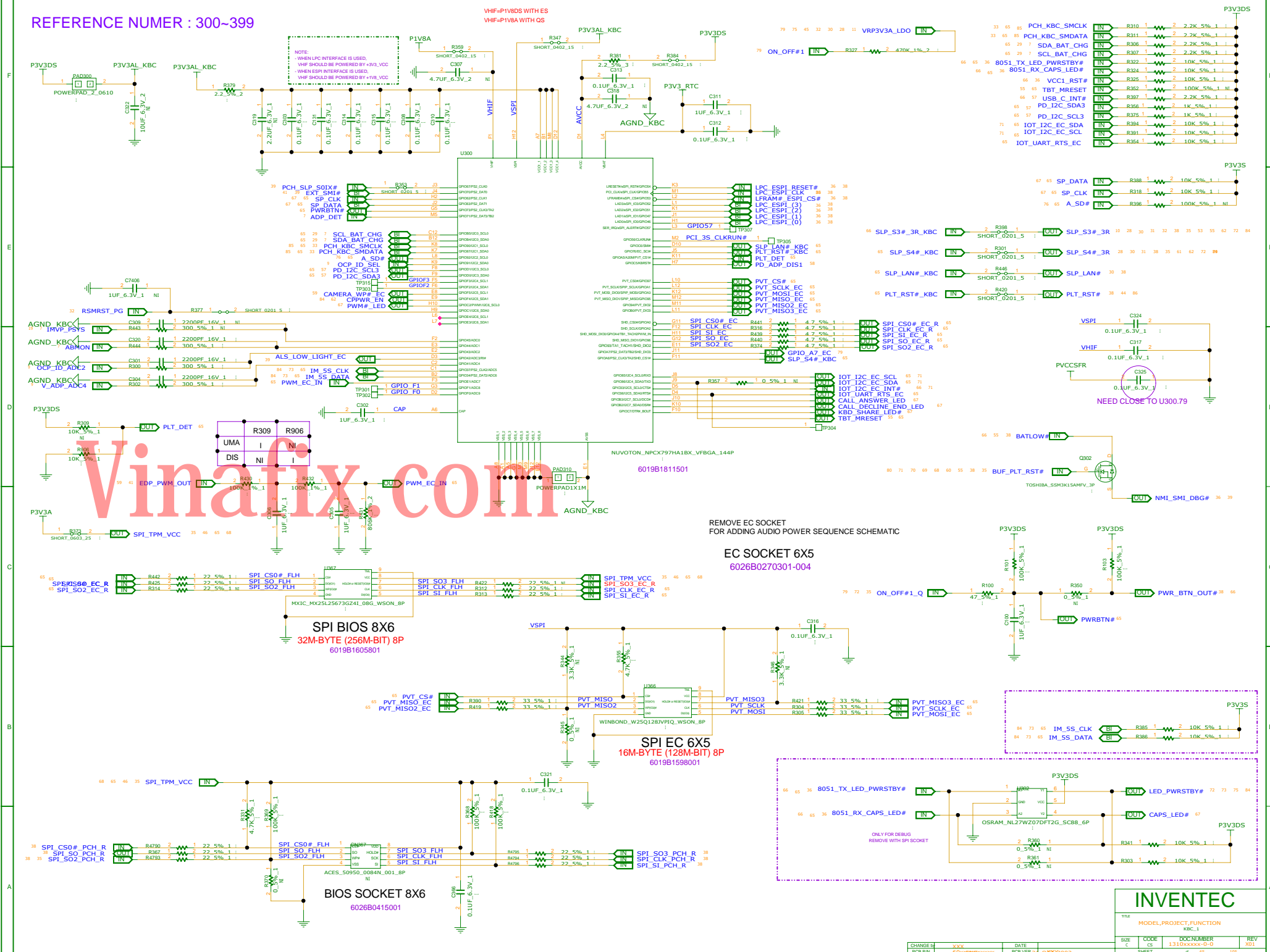
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		64 of 105	

CHANGE by PCB P/N	DATE PCB VER	21-OCT-2002 XXX
----------------------	-----------------	--------------------

REFERENCE NUMBER : 300~399

VHIF=P1V8DS WITH ES

VHIF=P1V8A WITH QS



REMOVE EC SOCKET
FOR ADDING AUDIO POWER SEQUENCE SCHEMATIC

EC SOCKET 6X5
6026B0270301-004

SPI BIOS 8X6
32M-BYTE (256M-BIT) 8P
6019B1605801

SPI EC 6X5
16M-BYTE (128M-BIT) 8P
6019B1598001

BIOS SOCKET 8X6
6026B0415001

INVENTEC

CHANGES	XXX	DATE	DATE	DATE	DATE
PCB PIN	PCB VER	PCB VER	PCB VER	PCB VER	PCB VER
SIZE	CODE	DOC NUMBER	REV		
SHEET	#	65	145		

D

C

B

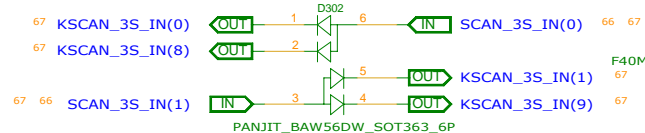
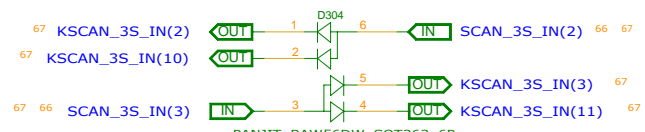
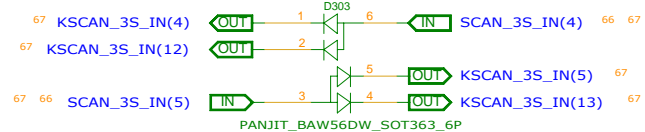
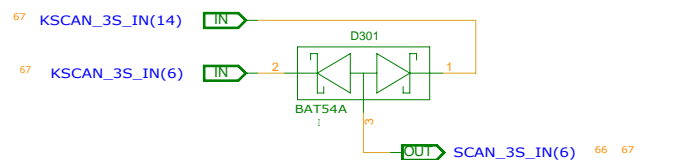
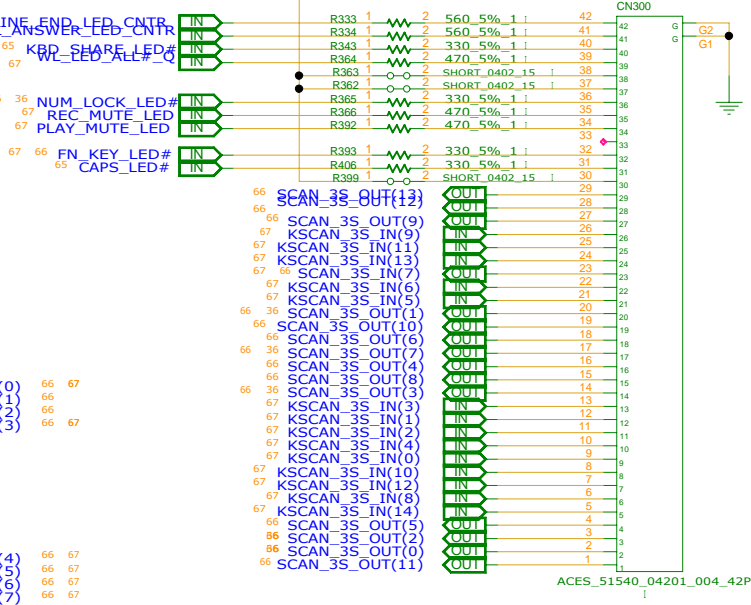
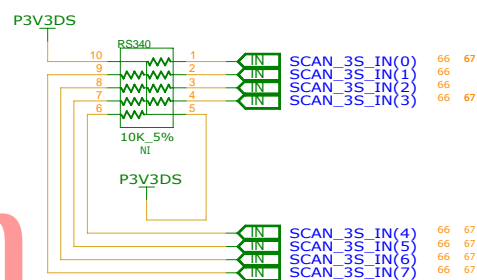
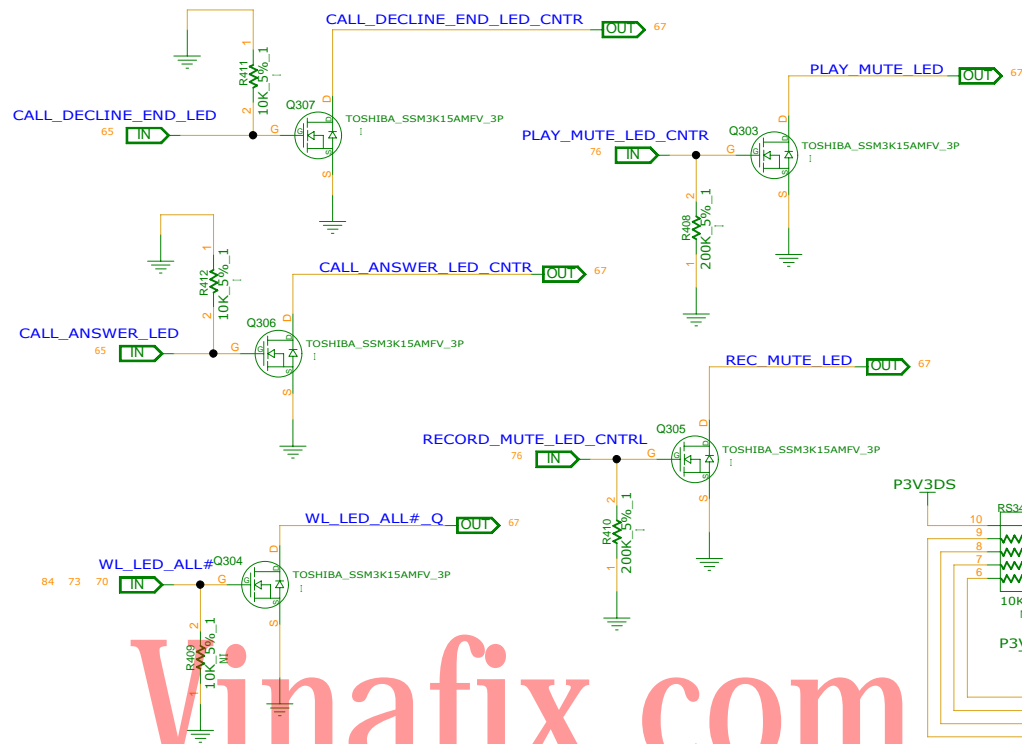
A

D

C

B

A

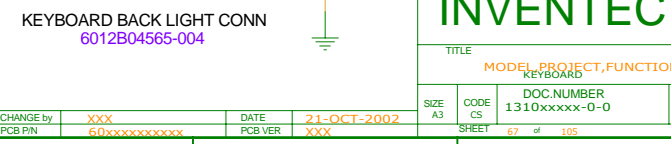
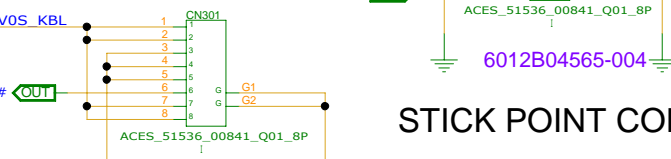
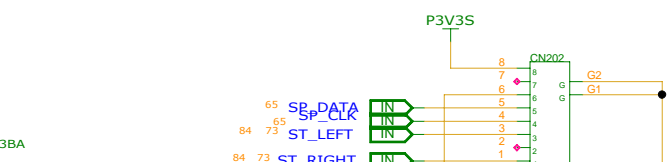
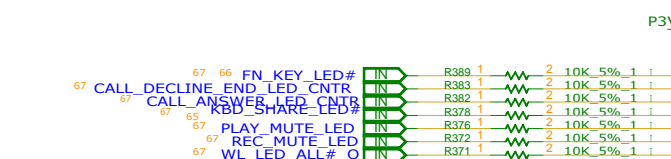


LOCATION NUMBER:400~499

6052B0295601

6052B0295601

6052B0295601



STICK POINT CONN

INVENTEC

MODEL PROJECT,FUNCTION

KEYBOARD

DOC NUMBER

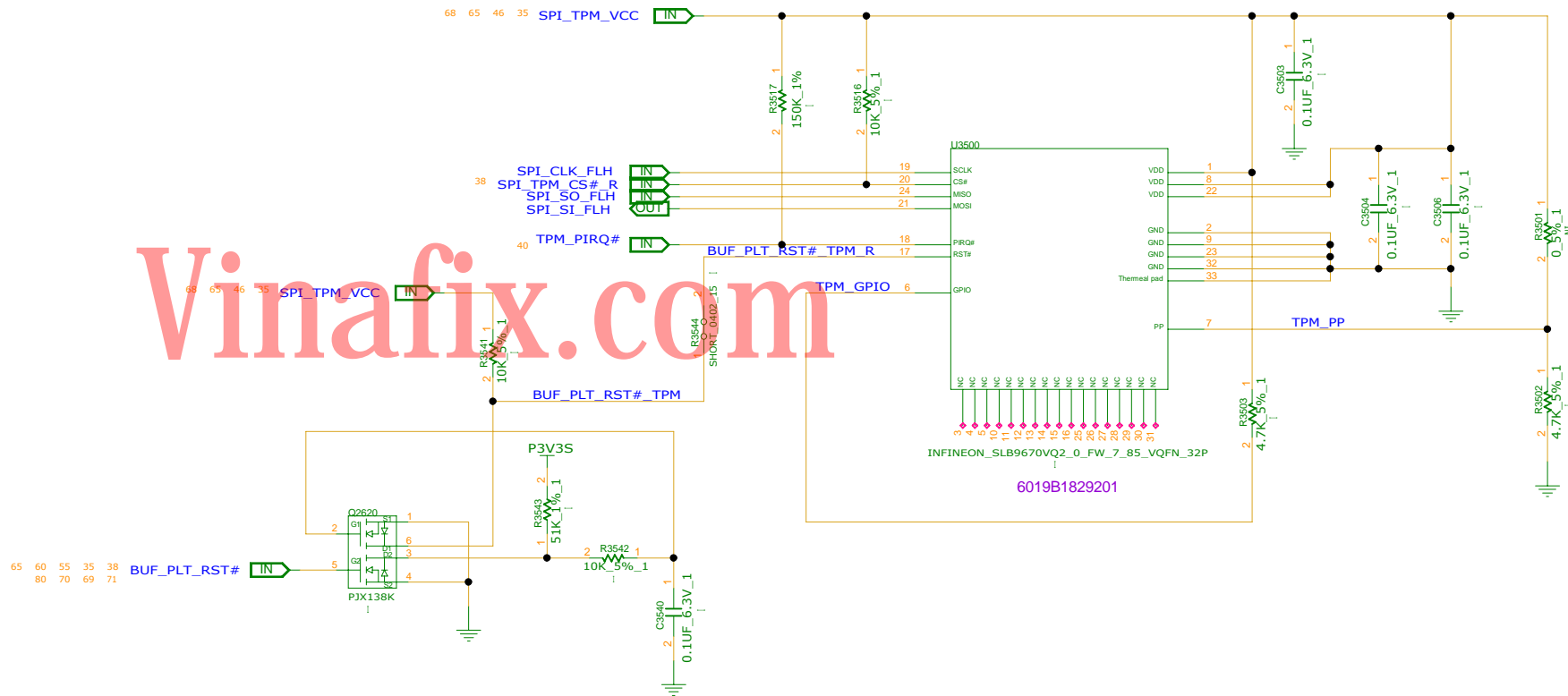
1310xxxxx-0-0

REV

X01

CHANGE by	DATE	PCB P/N	PCB VER	SHEET	of	105
XXX	21-OCT-2002	60xxxxxxx	XXX	67		

TPM2.0



LOCATION NUMBER:3500~3599

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 68 of 105

CHANGE by	DATE
XXX	21-OCT-2002

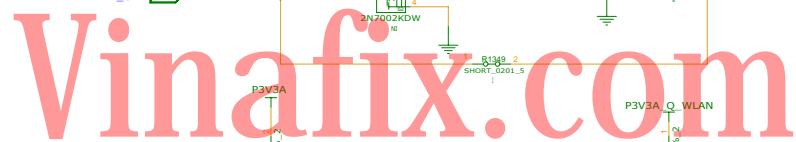
PCB P/N 60xxxxxxxxxxx PCB VER XXX

A	B	C	D	E	F
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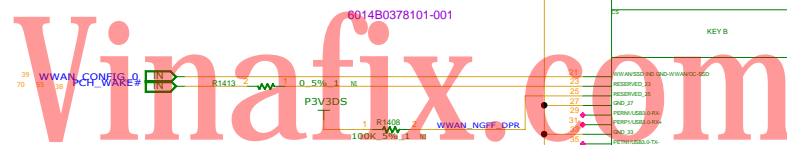
A

131605251103		300cd		765006		164		6		5		4		3		2		1	
PLB PIN		XXXXXXXXXXXX		PLB TER		XXXX		SHEET		OF		=		102					



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TITLE			
MODEL,PROJECT,FUNCTION WLAN			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		70	of 105



ST1400
STANDOFF_3.2_6.0
2.33MM
6052B0407701
WWAN
STANDOFF

CHANGE by	xxx	DATE	21-OCT-200
PCB P/N	60xxxxxxxxxxx	PCB VER	xxx

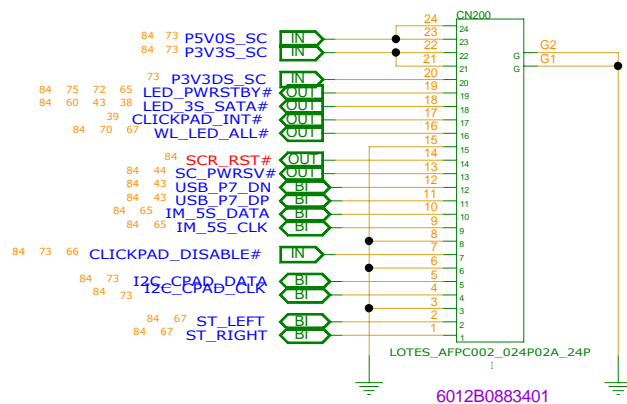


INVENTEC

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		72 of 105	

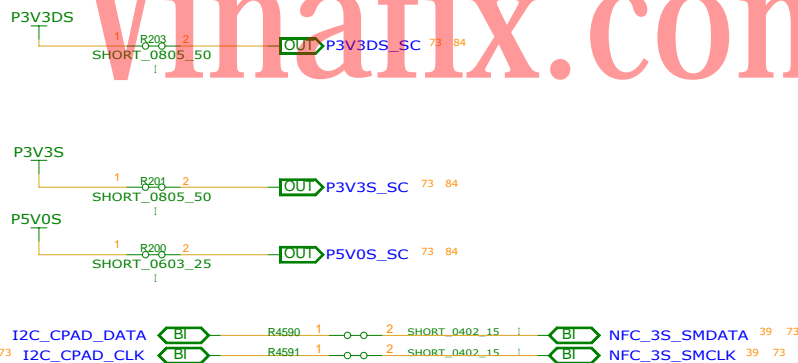
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

D



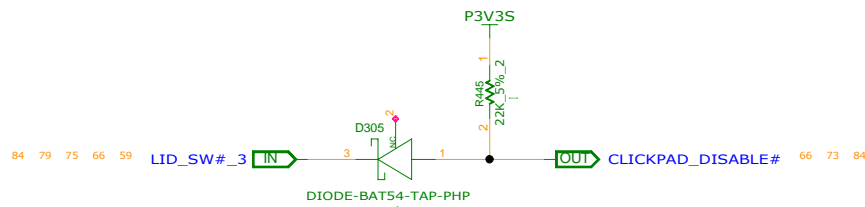
SMARTCARD CONN

NOTE : CONNECT TO CN9000 (P.79)
SMART CARD AND TOUCHPAD D/B W TO B CONN

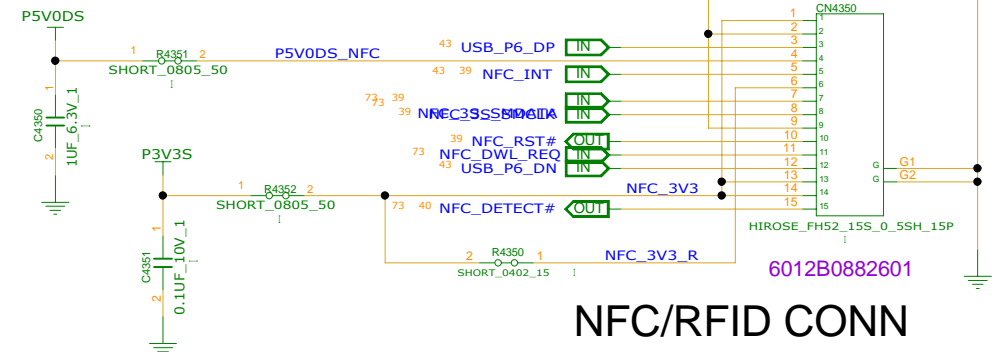


LOCATION NUMBER:850~999

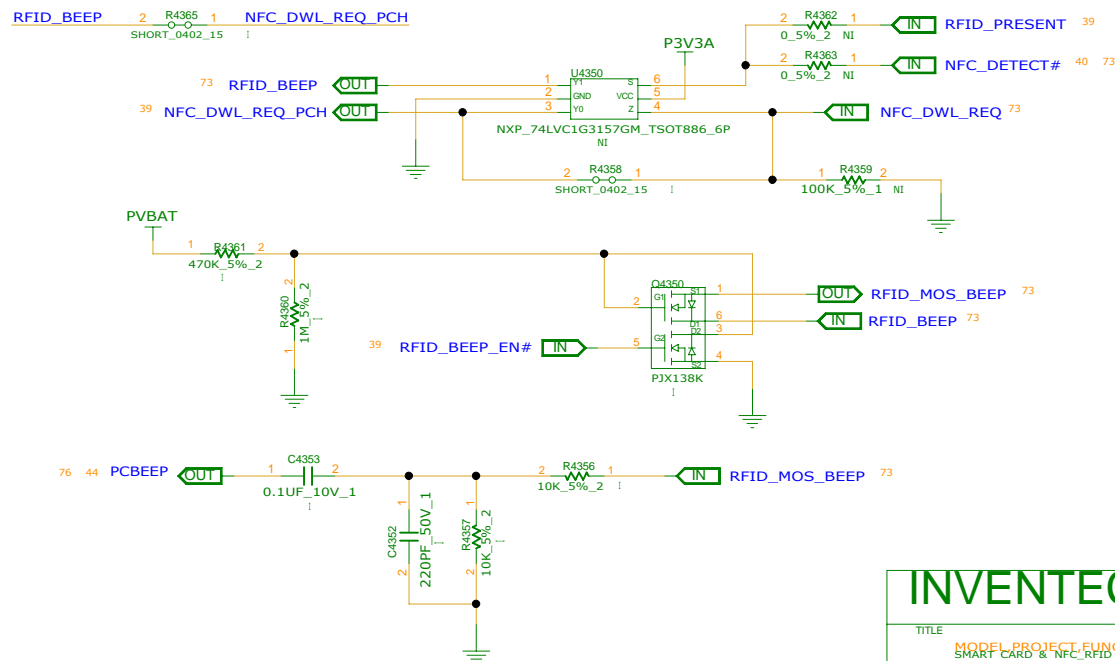
A



NFC	RFID	PIN
3.3V	NC	1
GND	GND	2
USB D+	USB D+	3
5V	5V	4
NFC_INT	CARD READ (O)	5
I2C_DATA	NC	6
I2C_CLK	NC	7
GND	GND	8
NFC_RST#	LOW POWER MODE (I)	9
NFC_DWL_REQ	AUDIO FEEDBACK BEEP (O)	10
USB D-	USB D-	11
3.3V	NC	12
3.3V	NC	13
NFC_DETECT#	RFID_DETECT	14



NFC/RFID CONN

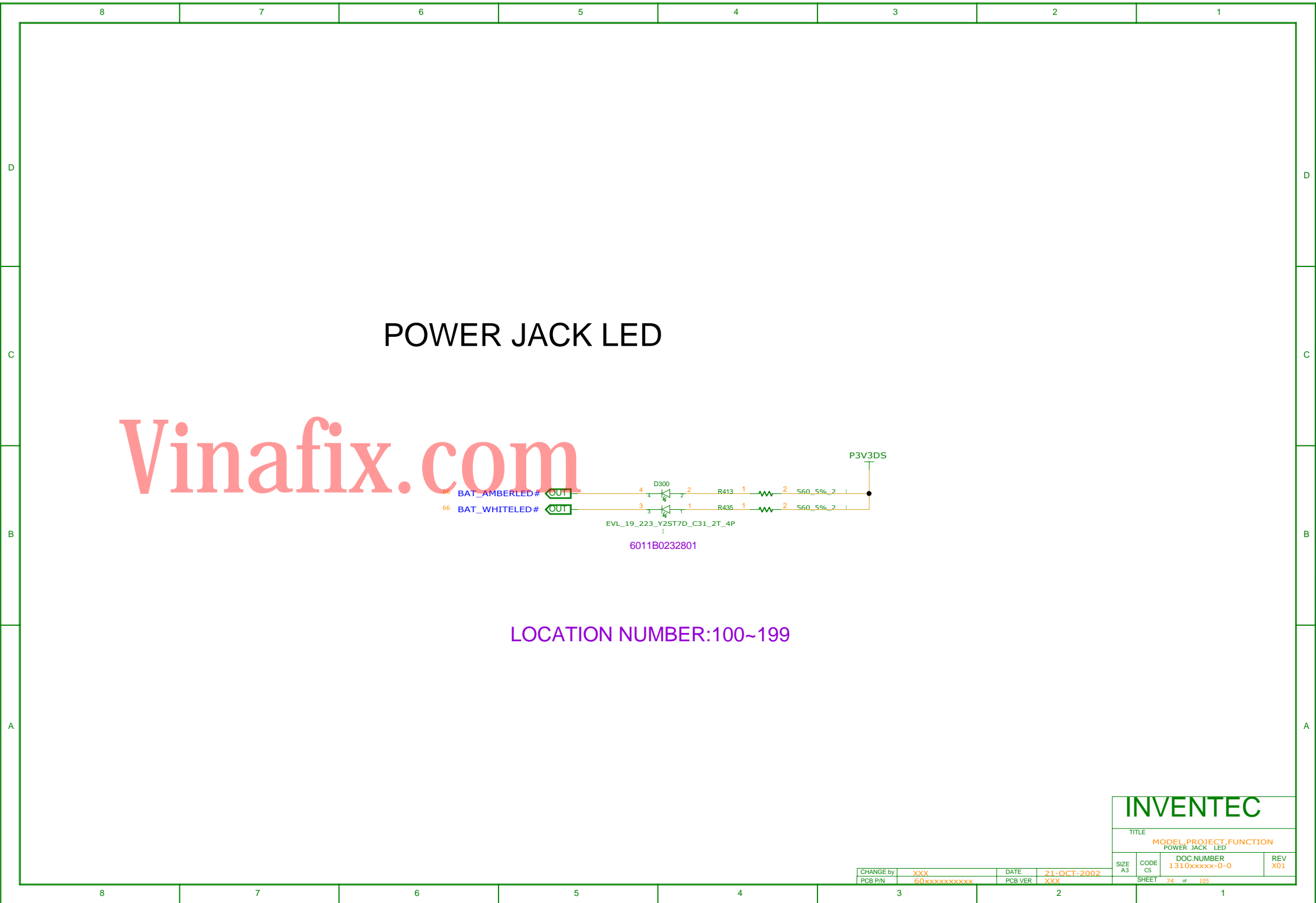


LOCATION NUMBER:4350~4399

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
SMART CARD & NFC/RFID			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		73 of 105	

CHANGE by	DATE
PCB P/N	PCB VER
XXX	21-OCT-2002
60xxxxxxxxxxx	XXX



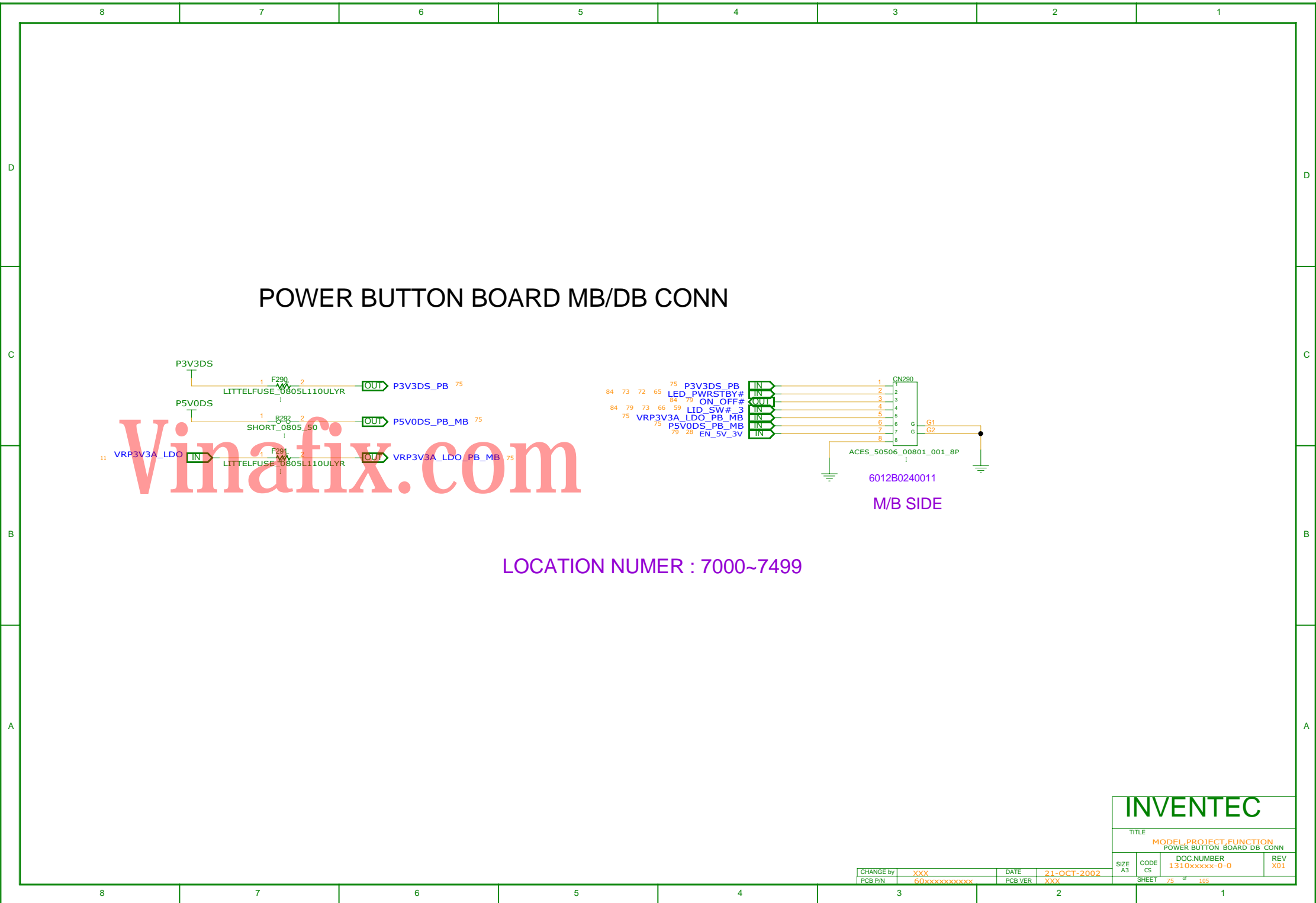
POWER JACK LED

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LOCATION NUMBER:100~199

INVENTEC			
TITLE MODEL PROJECT FUNCTION POWER JACK LED			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 74 of 105			

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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POWER BUTTON BOARD MB/DB CONN

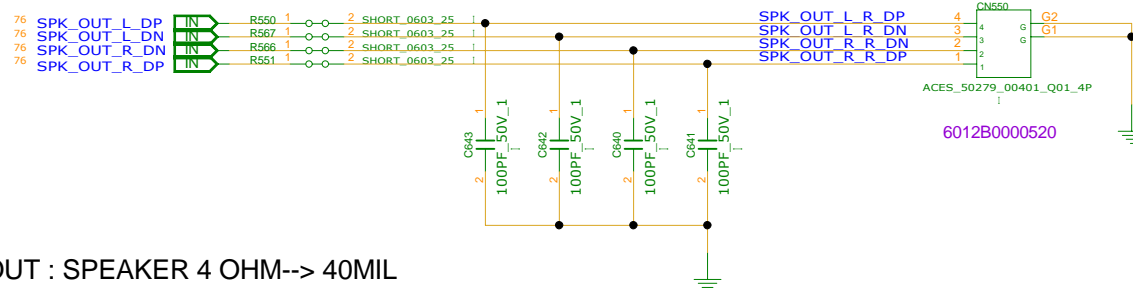
LOCATION NUMER : 7000~7499

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION POWER BUTTON BOARD DB CONN			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 75 of 105			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
AUD10		CODEC		
SIZE	CODE	DOC NUMBER		REV
A3	CS	1310XXXXXX-0-0		X01
SHEET		76	of	105



INTERNAL SPEAKER

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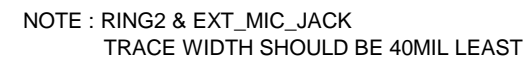
REFERENCE NUMBER:600~649



INVENTEC



TITLE
MODEL PROJECT,FUNCTION
SPEAKER

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		77 of 105	

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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76 HP_OUT_L_L1  1 R527 2 HP_OUT_R_L1 1 R534 2  HP_OUT_R_R_L1 78
30_5%_2 SHORT_0402_15

76 HP_OUT_R_L1  1 R531 2 HP_OUT_R_R_L1 1 R533 2  HP_OUT_R_R_R_L1 78
30_5%_2 SHORT_0402_15

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		78 of 105	

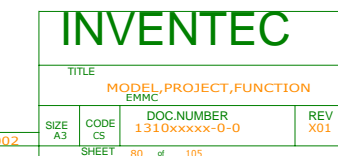
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE		MODEL PROJECT, FUNCTION	
		125 SHUT DOWN	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	
SHEET		79 of 105	

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCR P/N	60xxxxxxxxxx	PCR VER	XXX			SHEET	79	of 105	



LOCATION NUMBER : 1800~1899

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCR P/N	60xxxxxxxxxx	PCR VER	XXX			SHEET	80	of 105	

D

C

B

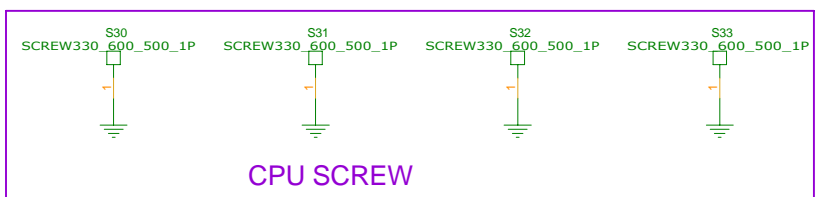
A

D

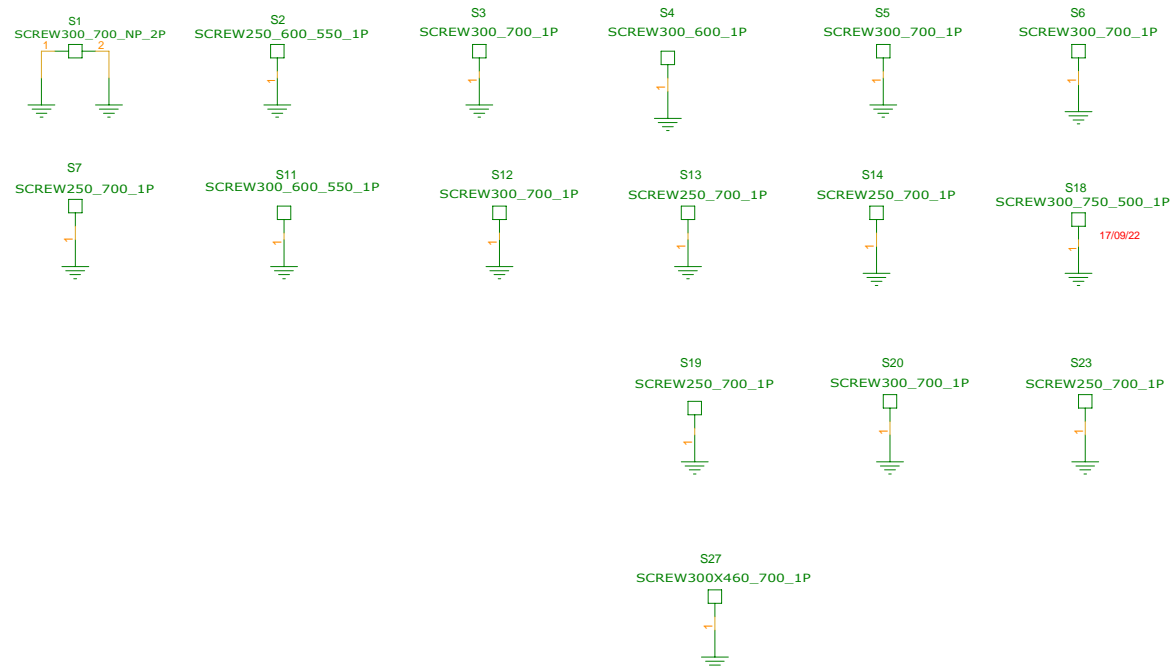
C

B

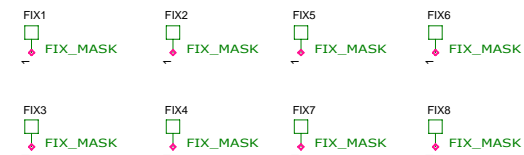
A



CPU SCREW



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LOCATION NUMER : S0~S49
ST0~ST49

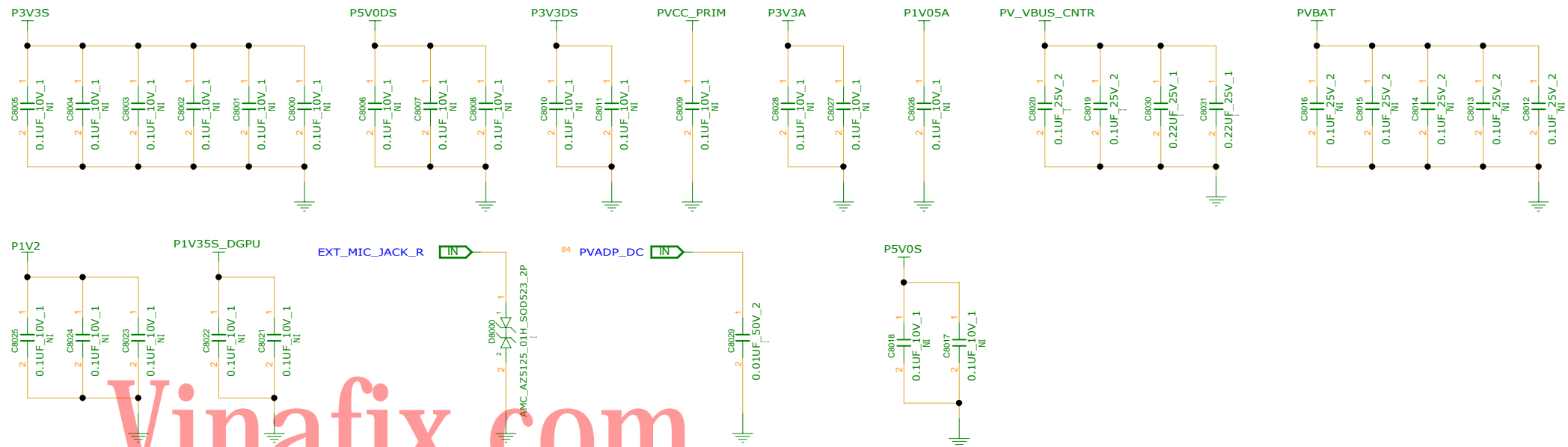
INVENTEC

TITLE
MODEL PROJECT,FUNCTION
SCREW

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		81 of 105	

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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EMI SOLUTION



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LOCATION NUMER : 8000~8199

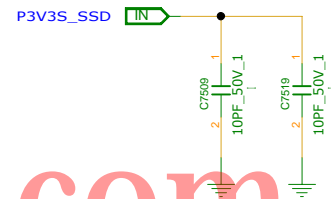
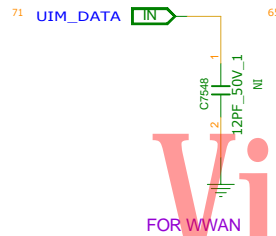
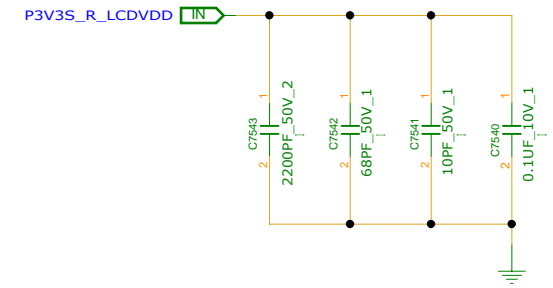
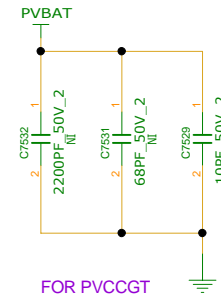
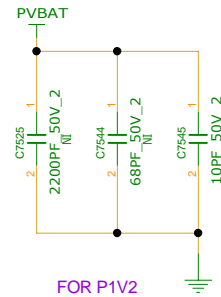
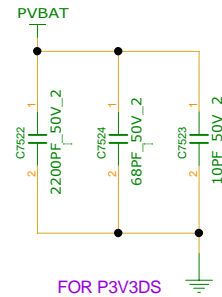
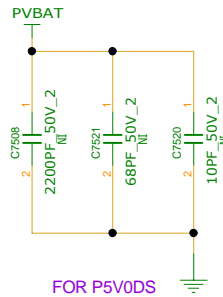
INVENTEC

TITLE
MODEL PROJECT,FUNCTION
EMI SOLUTIONSIZE
A3CODE
CSDOC NUMBER
1310xxxxx-0-0REV
X01CHANGE by
PCB P/NDATE
21-OCT-2002PCB VER
XXXSHEET
82 of 105

RF SOLUTION

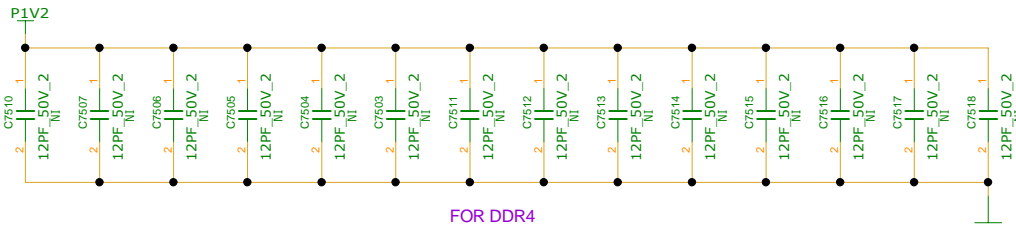
PAD7501
SMDPAD1_118X118_NP

RF FOR WWAN SOLUTION
NEED ADD UNDER THE MODULE



PAD7500
SMDPAD1_197X197_NP

RF FOR WWAN SOLUTION
NEED ADD UNDER THE MODULE



LOCATION NUMER : 8000~8199

INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
RF SOLUTION			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 83 of 105			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

D

C

B

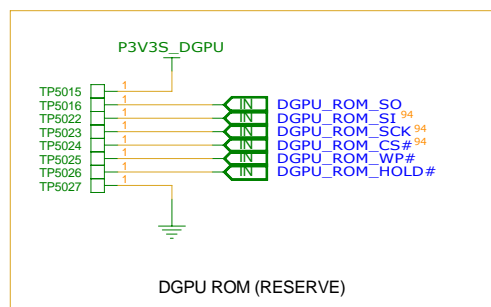
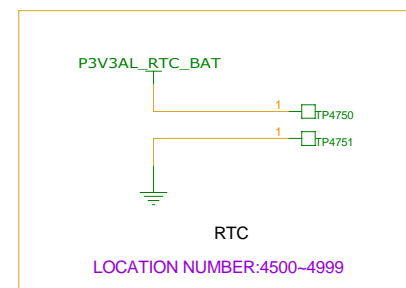
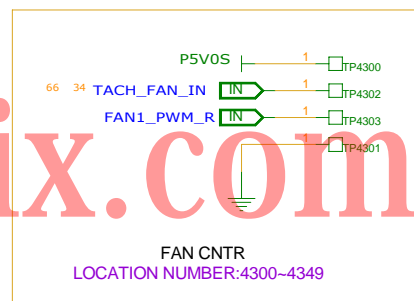
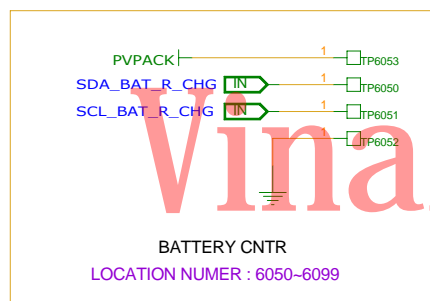
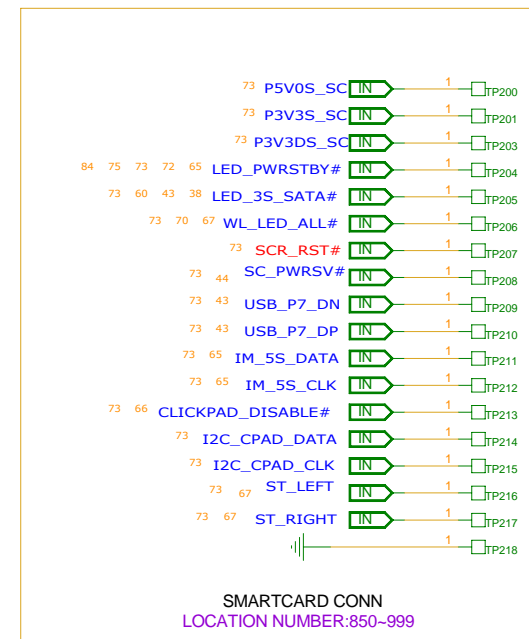
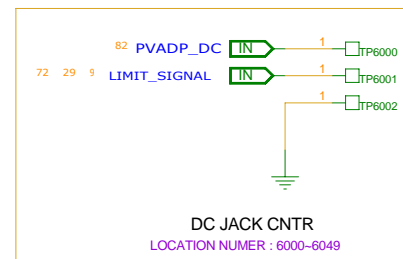
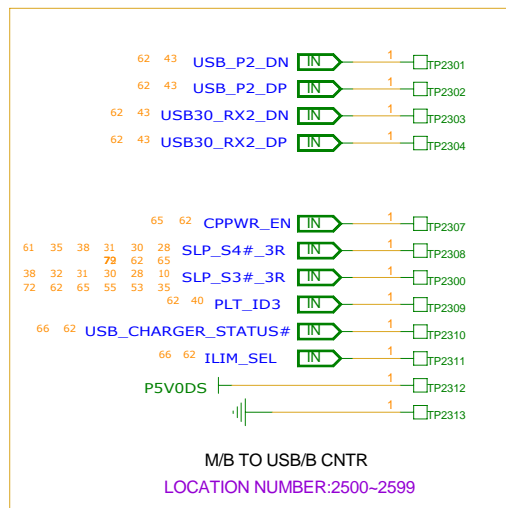
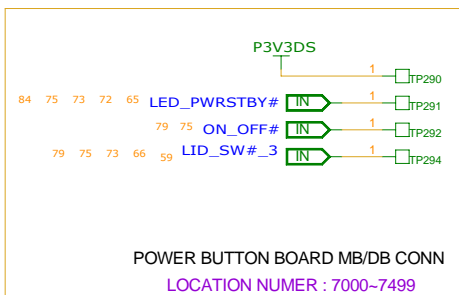
A

D

C

B

A



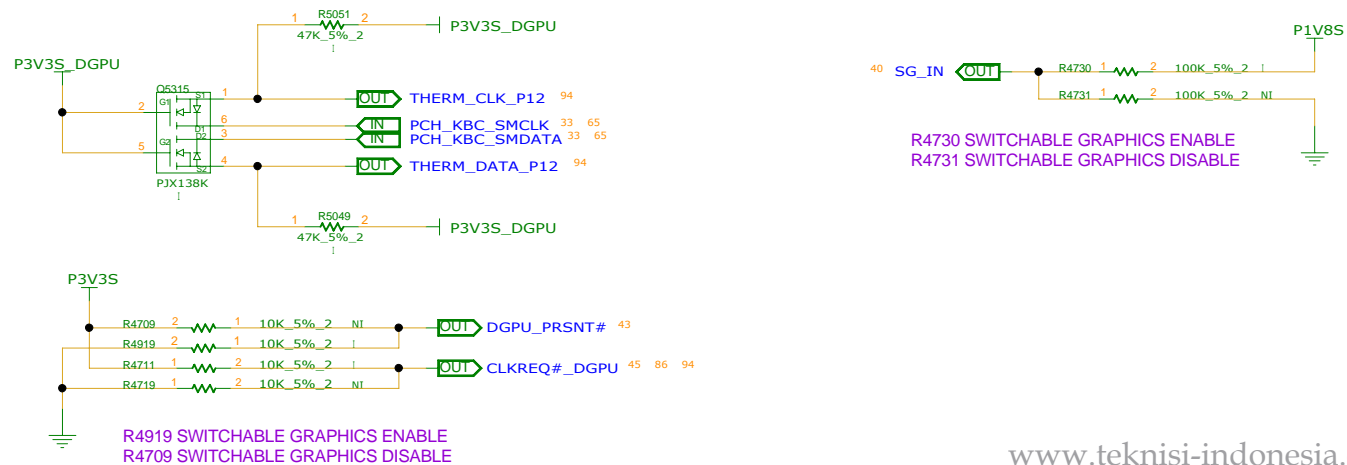
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TEST POINT

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 84 of 105

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FOR UMA MODE	
INSTALL	R4709 R4731 R309
UNINSTALL	Q5315 R4730 R4919 R906

INVENTECTITLE
MODEL PROJECT FUNCTION
DIS & UMA CHANGE PART

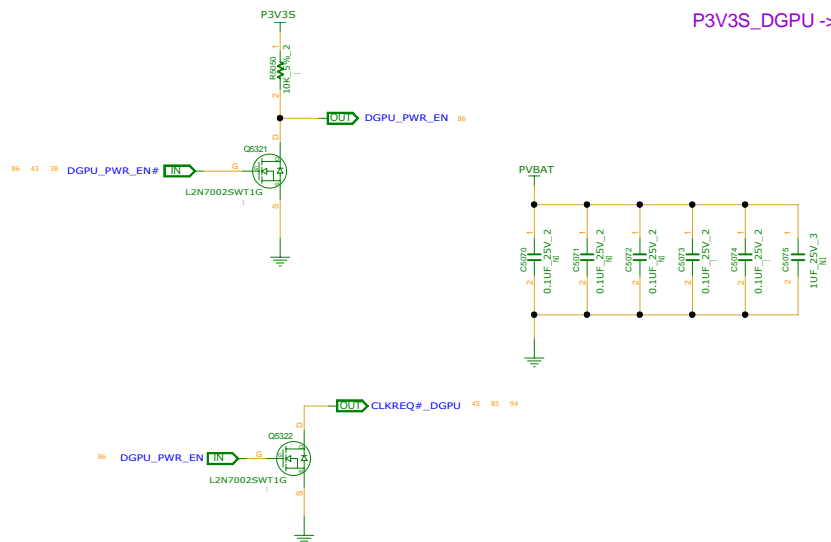
SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 85 of 105

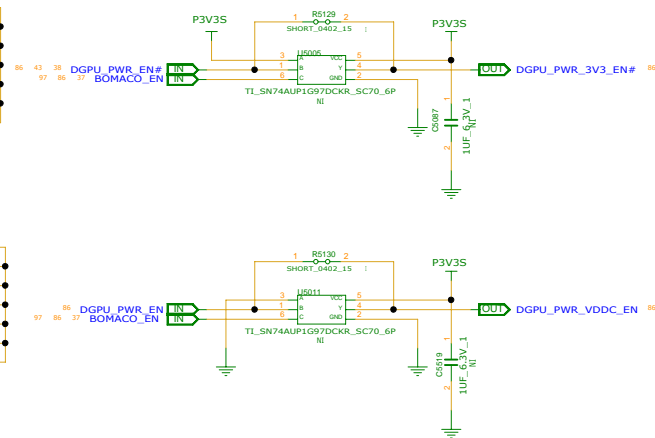
DGPU POWER SEQUENCE

P3V3S_DGPU -> P1V8S_DGPU -> PVCORE_DGPU & VDDCI -> P1V35S_DGPU

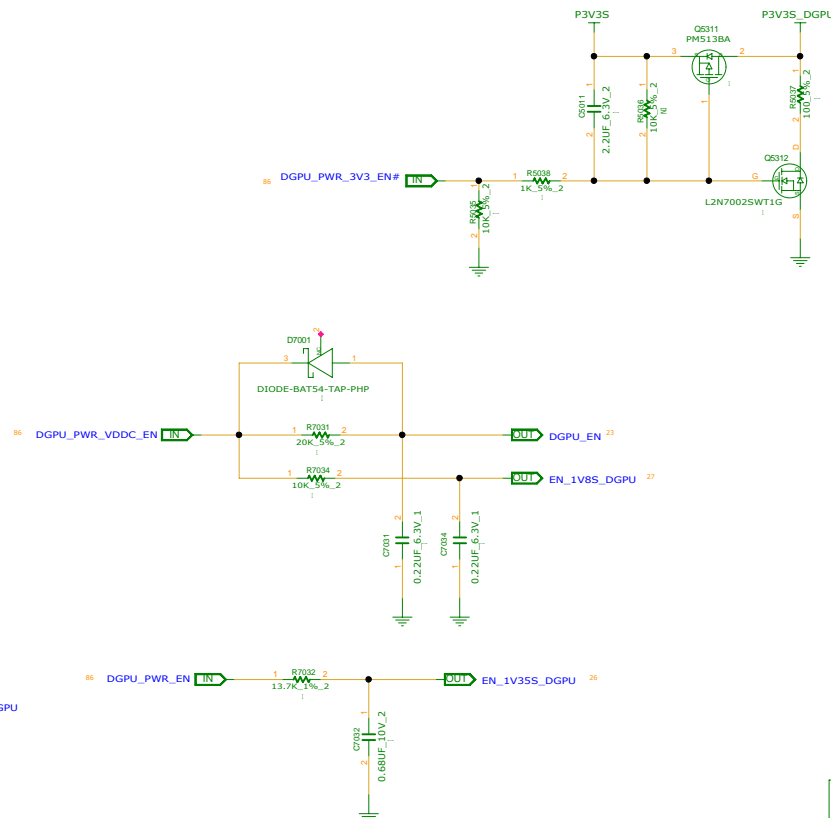
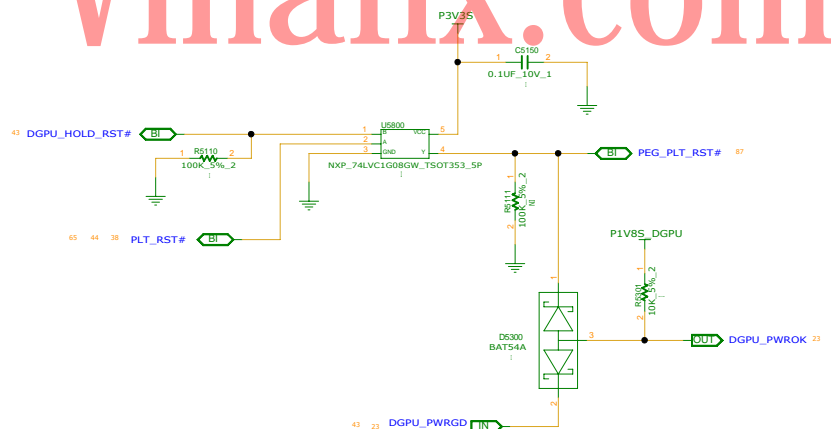


U5005				STATUS			
A	B	C	Y				
H	L	L	L	S0, HAVE DGPU, NO BAMAQO			
H	L	L	H	S0, NO DGPU, NO BAMAQO			
H	L	H	H	S0, HAVE DGPU, HAVE BAMAQO = MS MODE			
H	L	H	L	NC = NO DGPU, HAVE BAMAQO			

U5011				STATUS			
A	B	C	Y				
L	H	L	H	S0, HAVE DGPU, NO BAMAQO			
L	L	L	L	S0, NO DGPU, NO BAMAQO			
L	H	H	L	S0, HAVE DGPU, HAVE BAMAQO = MS MODE			
L	L	H	L	NC = NO DGPU, HAVE BAMAQO			



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FOR UMA MODE			
UNINSTALL	D7001	R7031	C7031
	C7032	R7034	C7034

INVENTEC

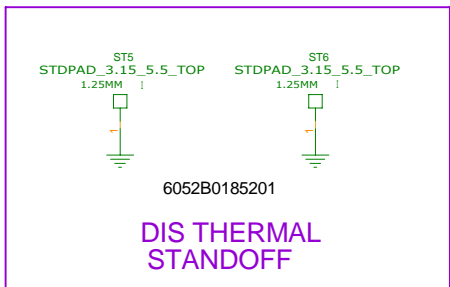
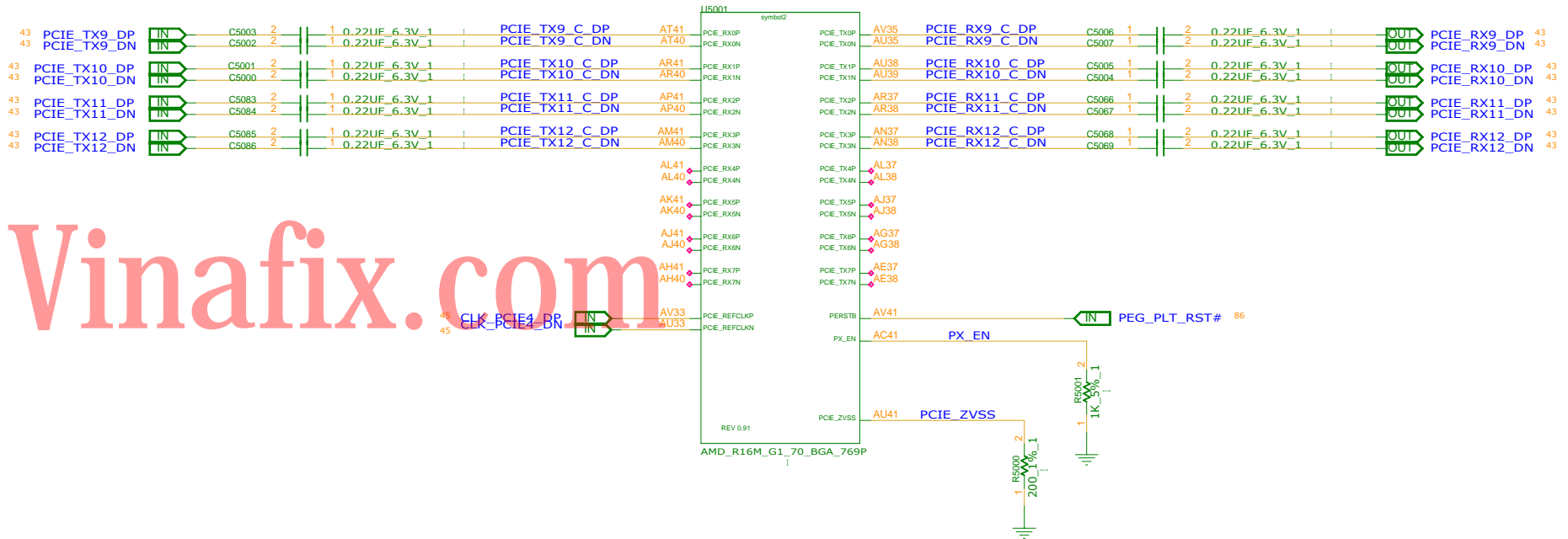
MODEL,PROJECT,FUNCTION
DGPU POWER SEQUENCE

SIZE CODE DOC NUMBER REV
A3 CS 1310XXXX-0-0 201

CHGNGR PCB PIN XXXXXXXXXXXX DATE 21-OCT-2002 PCB VER XXX

SHEET 10 100

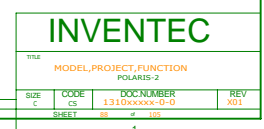
GPU PCI-E



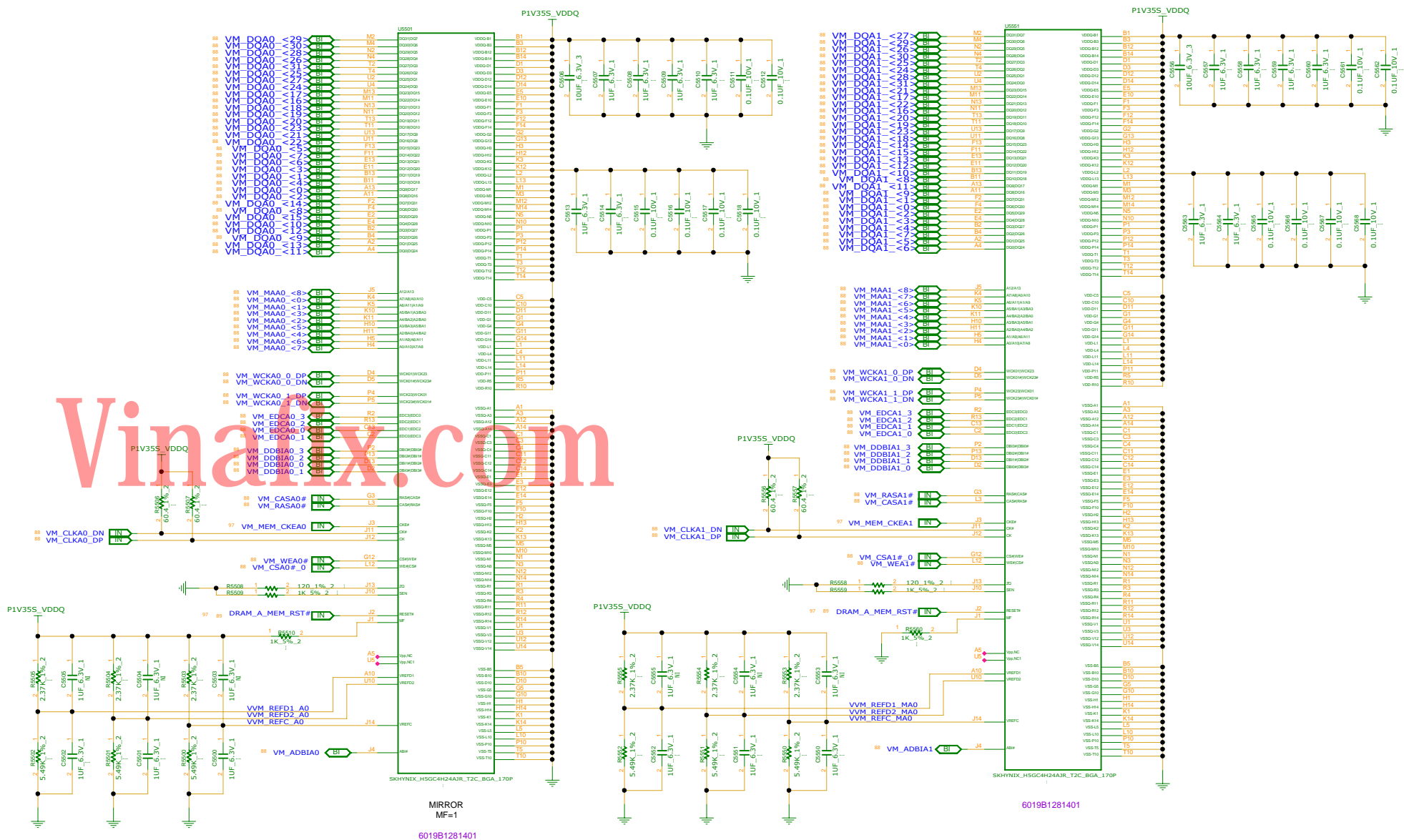
INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
POLARIS-1			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 87 of 105			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

GPU FRAME BUFFER B



VRAM A PARTITION



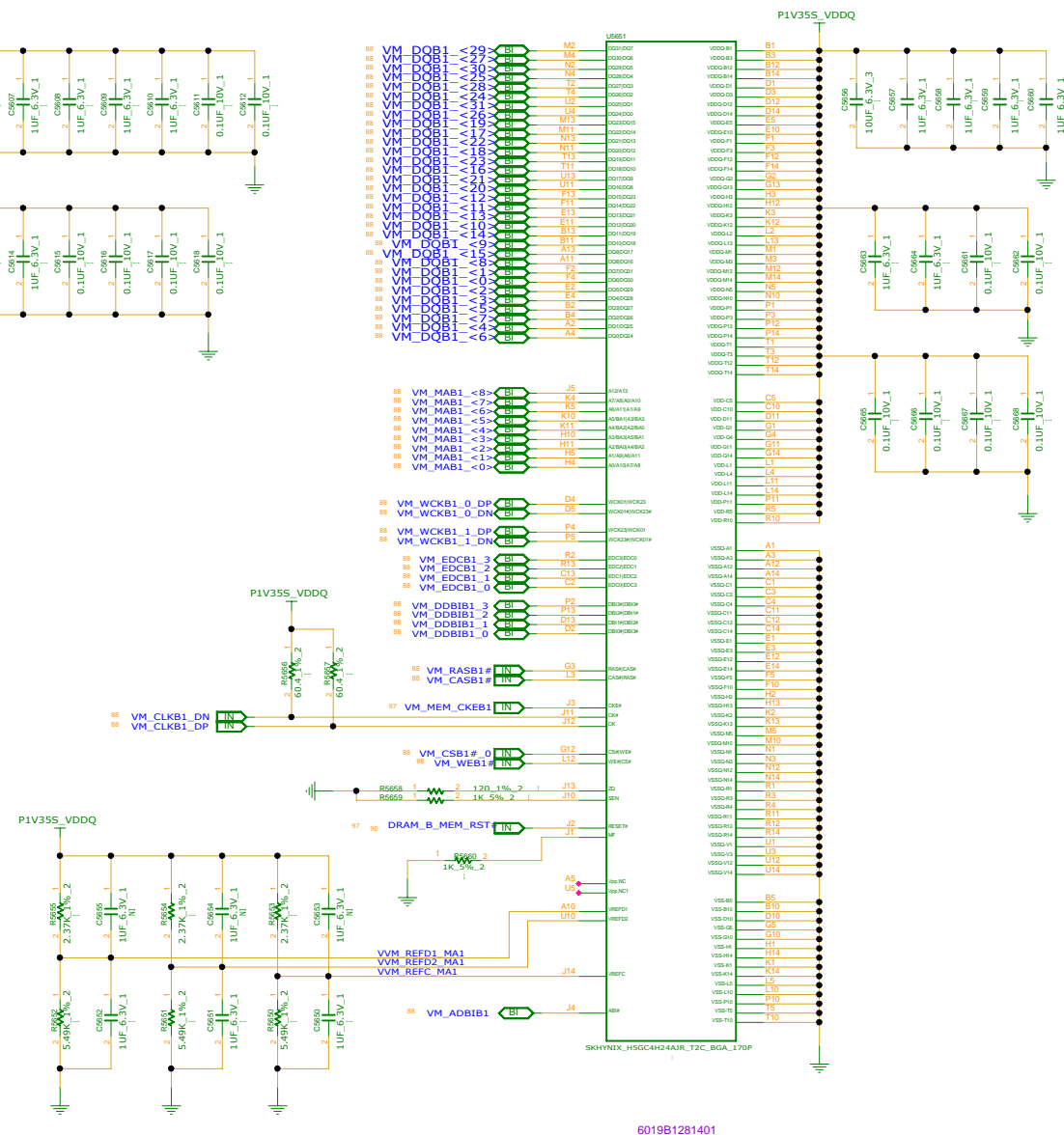
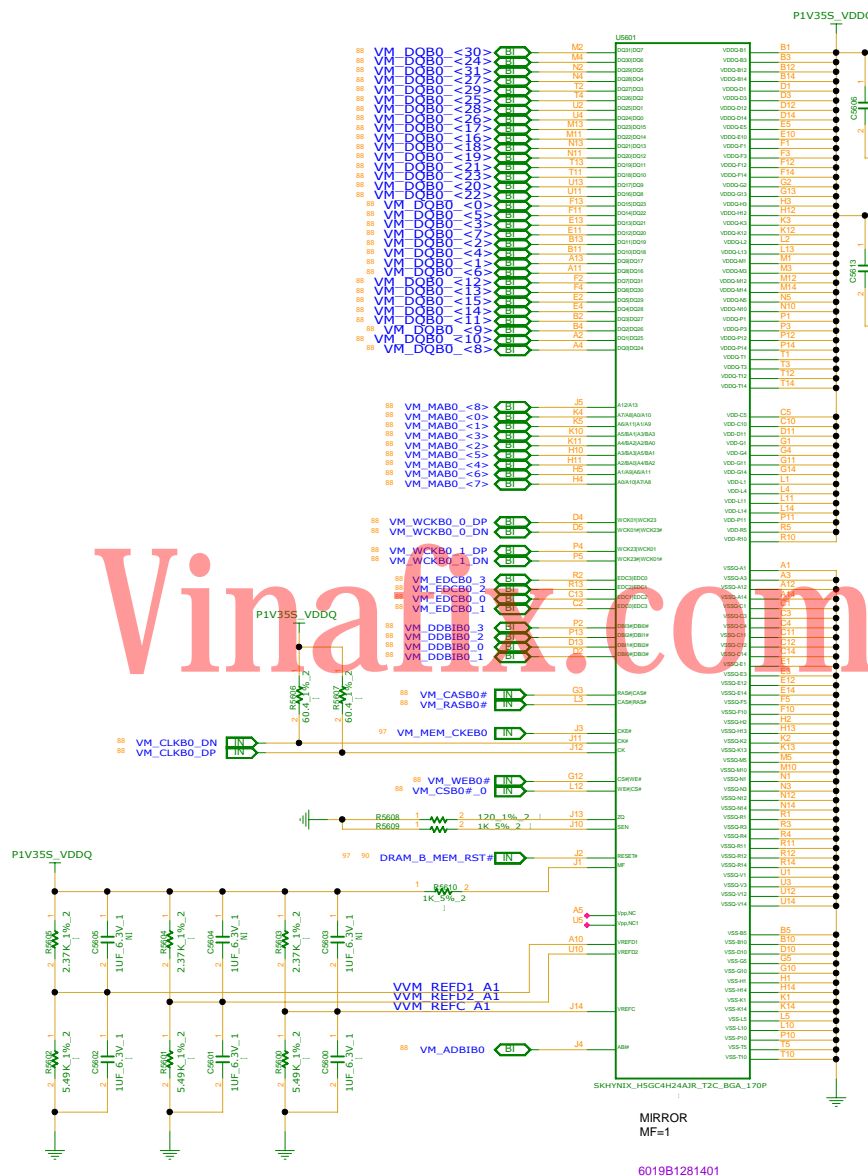
INVENTEC

MODEL,PROJECT,FUNCTION			
VRAM-1			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310VXXXXX-0-0	201
SHEET	REV	REV	REV
1	1	1	1

CHANGED	DATE	DATE
PCB PIN	21-OCT-2002	21-OCT-2002
PCB VER	1.0	1.0

VRAM B PARTITION

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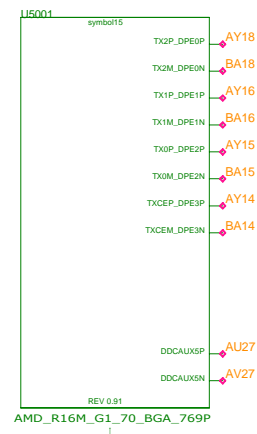
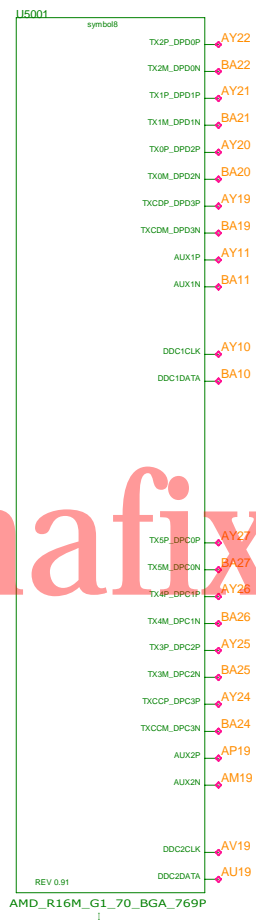


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
VRAM-2			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310VXXXXX-0-0	201
SHEET			
99 of 108			

CHANGED	DATE
XXX	21-OCT-2002
PCB PIN	PCB VER
6019B1281401	XXX

GPU VGA / LVDS / DVI / HDMI / DP



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INVENTEC

TITLE
MODEL PROJECT,FUNCTION
POLARIS-9

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

SHEET 91 of 105

CHANGE by	DATE
XXX	21-OCT-2002

PCB P/N 60xxxxxxxxxx PCB VER XXX

GPU-LVDS

Vinafix.com



INVENTEC

TITLE
MODEL PROJECT,FUNCTION
POLARIS-4

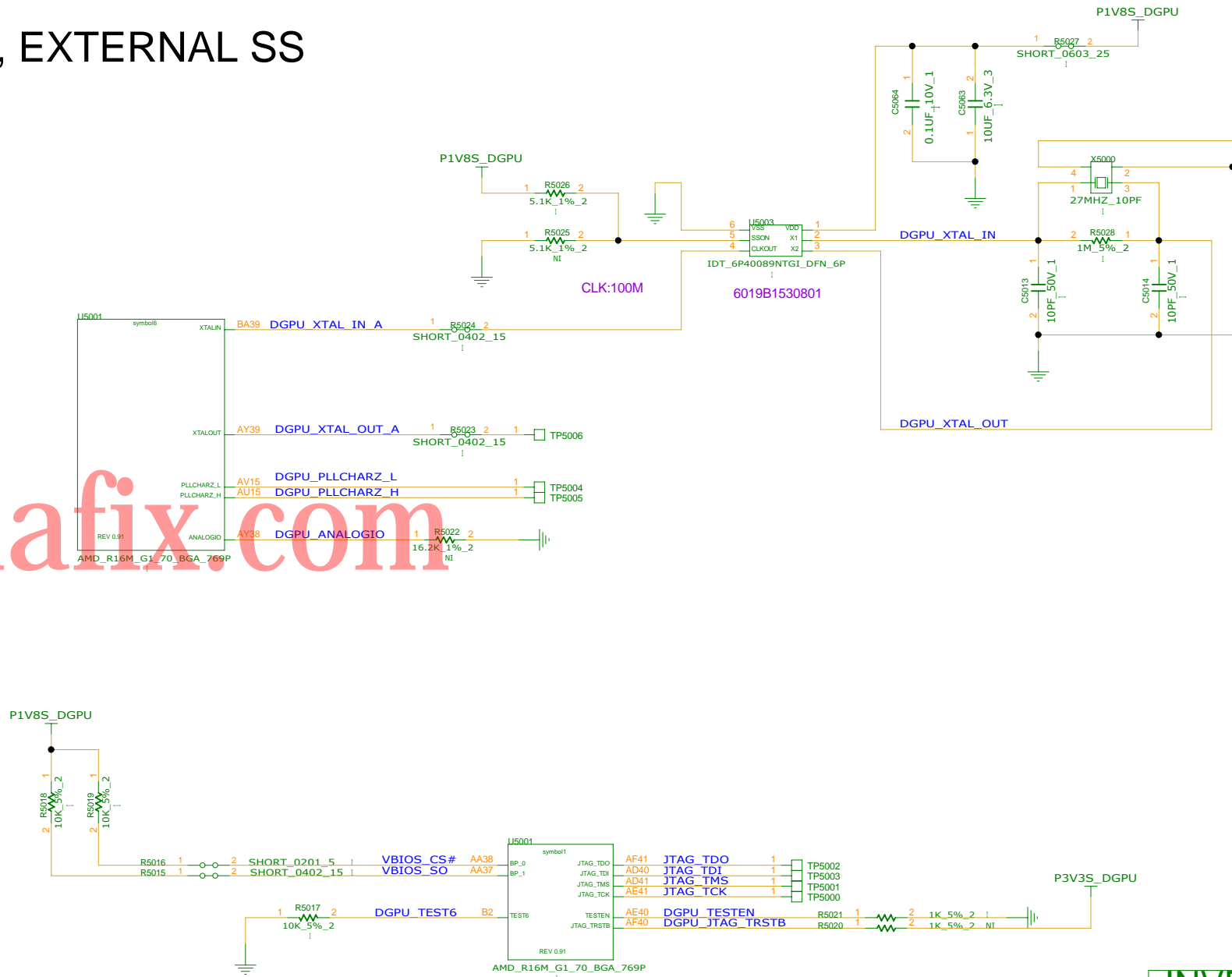
SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 92 of 105

GPU BIOS, EXTERNAL SS

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INVENTEC

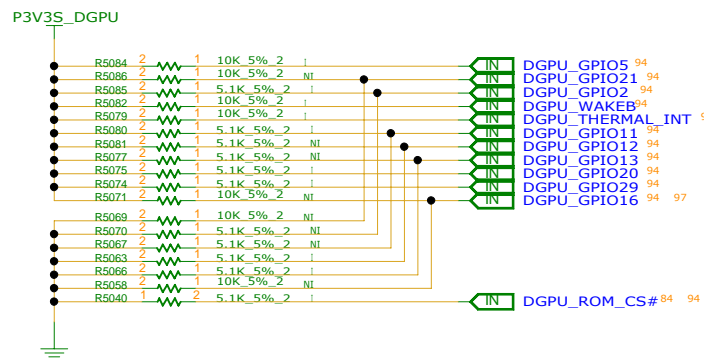
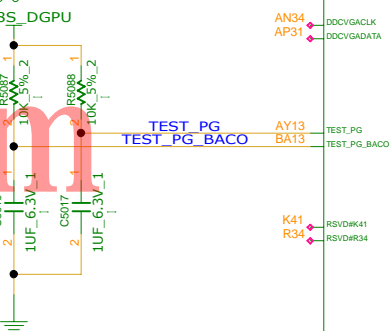
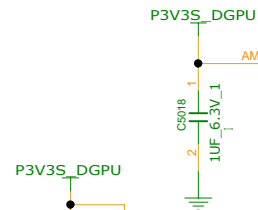
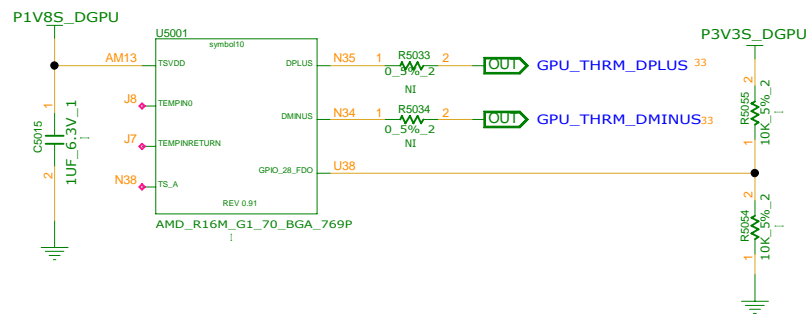
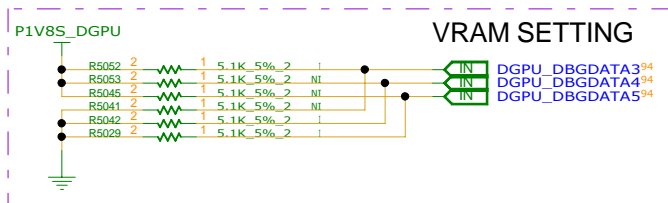
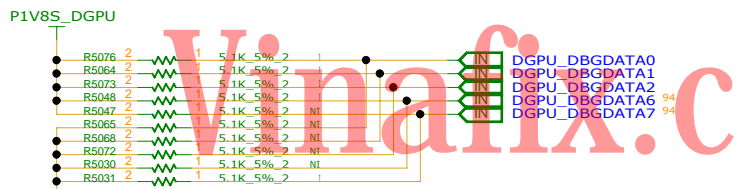
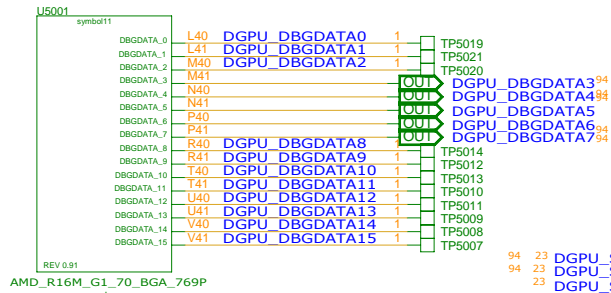
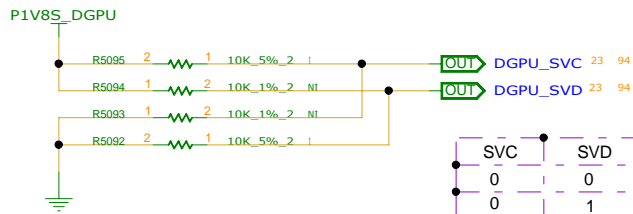
TITLE
MODEL PROJECT,FUNCTION
POLARIS-5SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01
SHEET 93 of 105CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

D

C

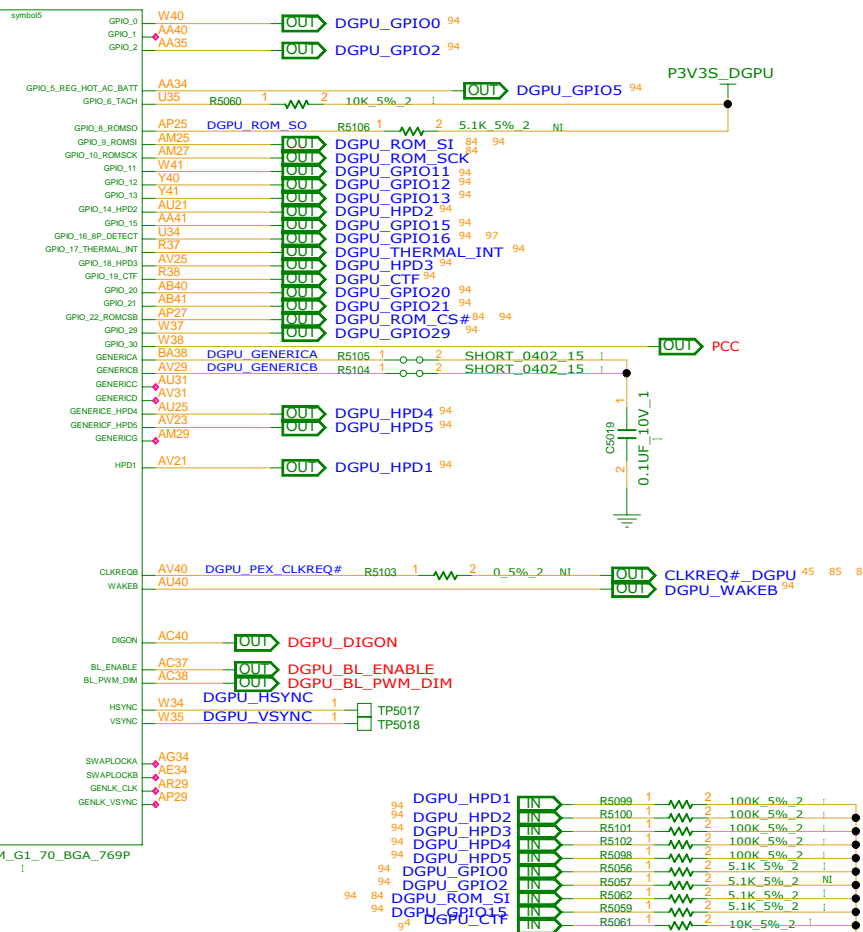
B

A



GPU-THERMAL /DEBUG

GPU GPIOs, I2C



teknisi indonesia

INVENTECTITLE
MODEL PROJECT,FUNCTION
POLARIS-6SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

SHEET 94 of 105

CHANGE by XXX
PCB P/N 60xxxxxxxxxxDATE 21-OCT-2002
PCB VER XXX

D

C

B

A

D

C

B

A

GFX POWER/GND

PVCORE_DGPU

PVDDCI_DGPU

P1V35S_DGPU

P1V8S_DGPU

P1V35S_DGPU

PVDDCI_DGPU

INVENTEC

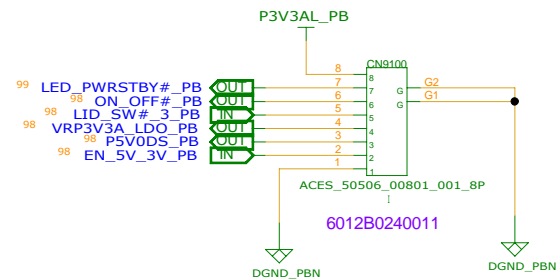
TITLE
MODEL PROJECT, FUNCTION
POLARIS-7SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01
SHEET 95 of 105CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

0 : 14" 0 : P series 01*11 : Reserved for discrete VRAM groups 0 : 256Mx32*2 (1 1 : 15" 1 : W series 1 : 256Mx32*4 (1

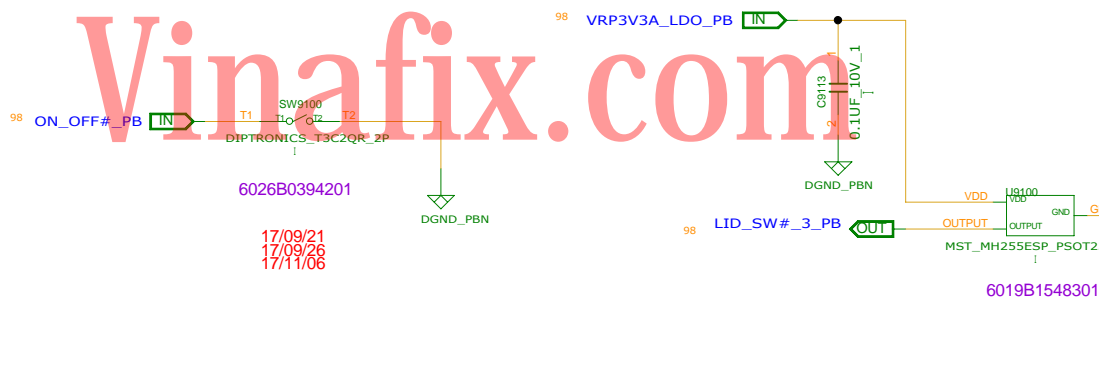
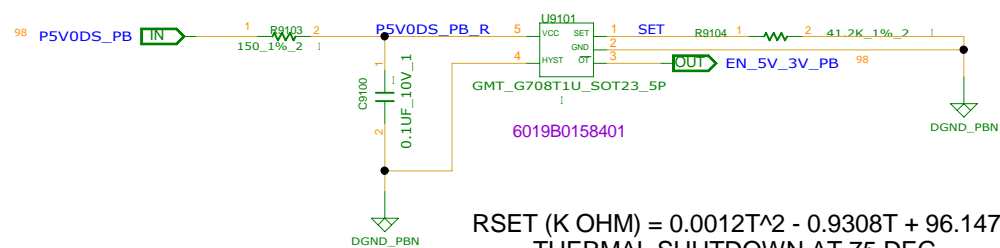
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



	STREET	27	-	103
			1	

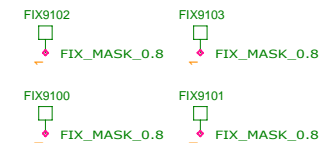
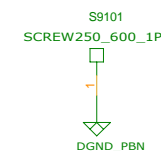


AMBIENT TEMP SENSE



POWER SWITCH DAUGHTER BOARD

LOCATION NUMBER:9000~9099



INVENTEC

TITLE			
MODEL PROJECT FUNCTION POWER BUTTON BOARD			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 98 of 105			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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D

C

B

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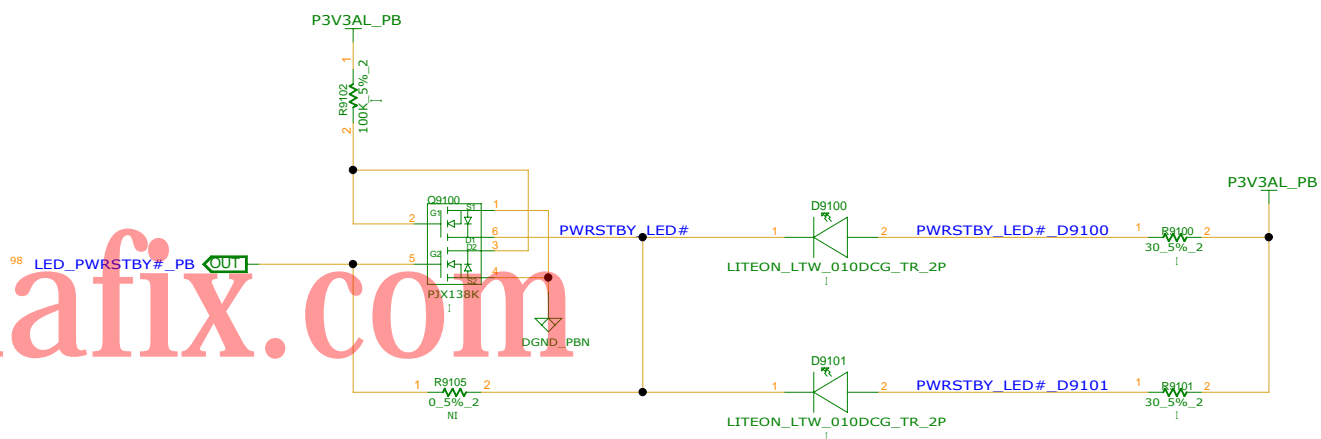
D

C

B

A

POWER BUTTON BOARD LED



LOCATION NUMBER:9000~9099

INVENTEC

TITLE
MODEL PROJECT FUNCTION
POWER BUTTON BOARD LED

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

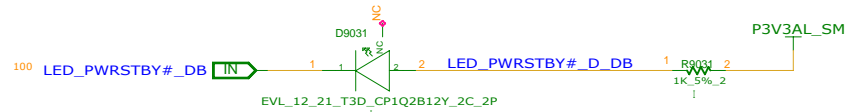
CHANGE by	DATE
XXX	21-OCT-2002
PCB P/N	PCB VER
60xxxxxxxxxxx	XXX

SHEET 99 of 105



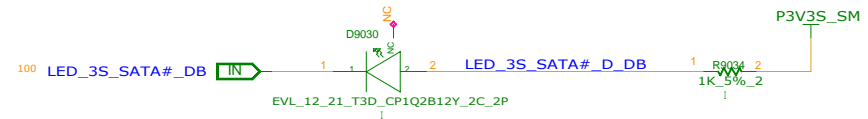
CHANGE by	xxx	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SMART CARD D/B LED



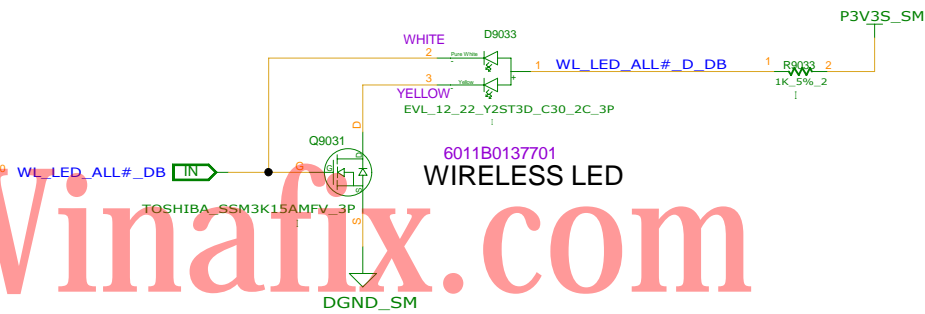
6011B0115101-005

POWER LED



6011B0115101-005

SATA LED

6011B0137701
WIRELESS LED

Vinafix.com

LOCATION NUMBER:9100~9199

INVENTEC

TITLE

MODEL PROJECT FUNCTION

SMART CARD DB LED

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		101 of 105	

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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D

C

B

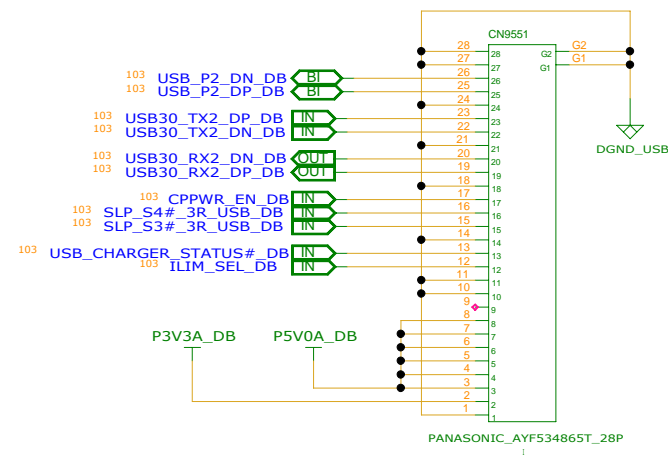
A

D

C

B

A



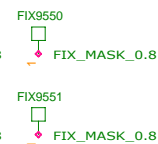
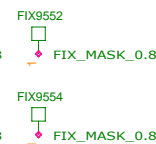
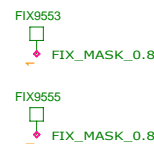
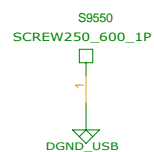
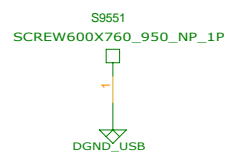
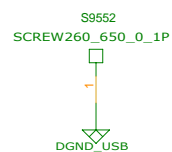
PANASONIC_AYF534865T_28P

6012B0440205-001

NOTE : CN9551.13 IS PLT_ID3, NOT GND

Vinafix.com

USB DB CNTR



LOCATION NUMBER:9200~9299

INVENTECTITLE
MODEL PROJECT,FUNCTION
USB DB CNTR

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 102 of 105



SIZE	CODE	1310xxxxx-0-0
A3	CS	
SHEET		103 of 105

D

C

B

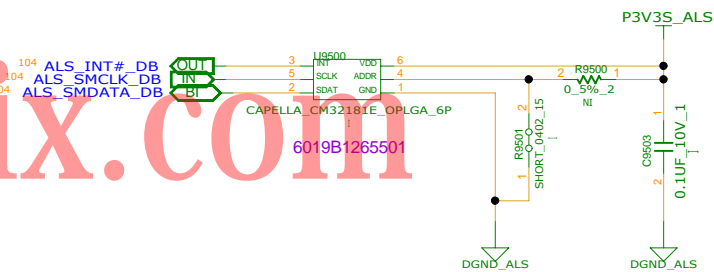
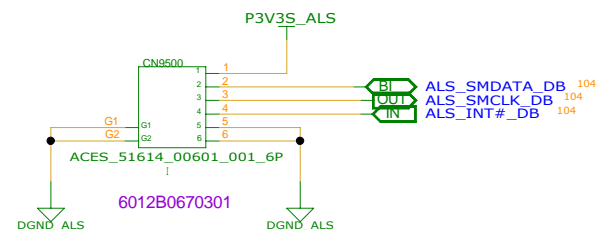
A

D

C

B

A



AMBIENT LIGHT SENSOR

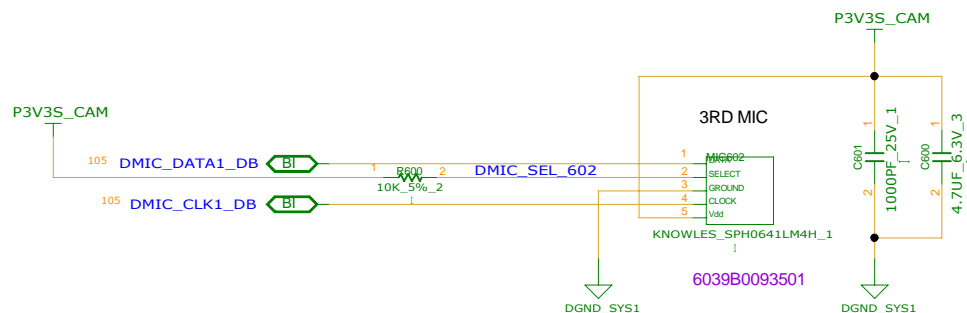
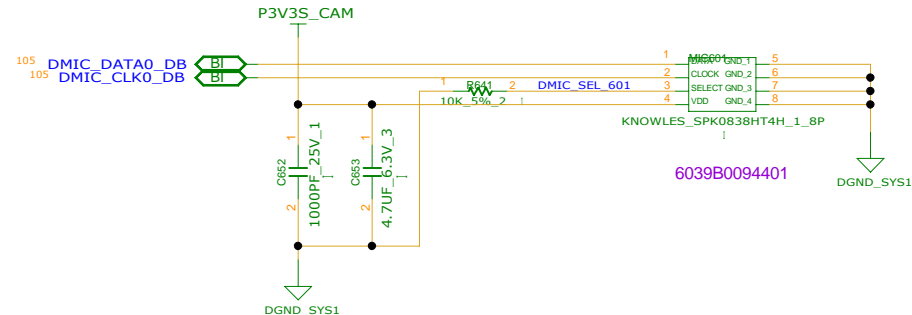
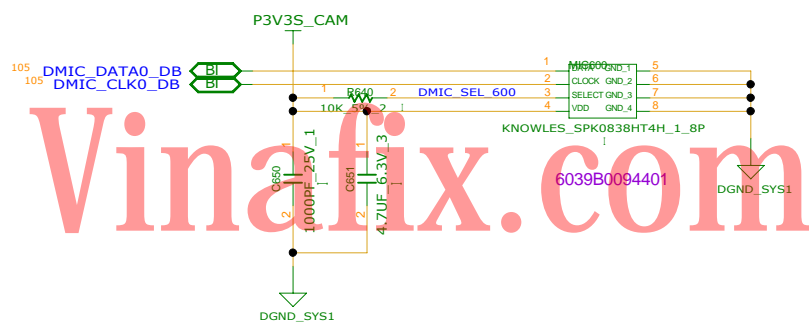
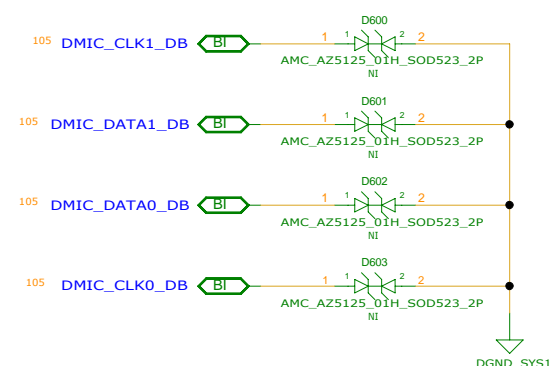
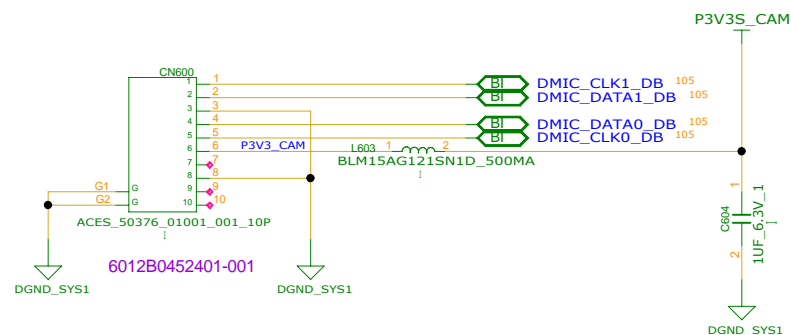
ADDR IS HIGH, SELECT ADDRESS 0X48
ADDR IS LOW, SELECT ADDRESS 0X10



LOCATION NUMBER:9300~9349

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

INVENTEC			
TITLE MODEL PROJECT,FUNCTION ALS D/B			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		104 of 105	



MIC DOUGHTER BOARD

LOCATION NUMBER:9350~9399



FIX_MASK_0.8



FIX_MASK_0.8

INVENTEC

TITLE MODEL PROJECT,FUNCTION

MIC BOARD

SIZE CODE DOC NUMBER REV

A3 CS 1310xxxxx-0-0 X01

SHEET 105 of 105

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX